PHILIPS

Data handbook

Philips Electronic components and materials

Integrated circuits

Book IC08N 1984
New series

ECL 10K and 100K logic families

NEW HANDBOOK SERIES

ECL 10K AND 100K LOGIC FAMILIES

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 50 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1 **Tubes for r.f. heating**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

T3 **Klystrons, travelling-wave tubes, microwave diodes**

ET3 **Special Quality tubes, miscellaneous devices** (will not be reprinted)

T4 **Magnetrons**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 **Camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicons and Newvicons**

T13 **Image intensifiers**

T14 **Infrared detectors**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2a **Power diodes**

S2b **Thyristors and triacs**

S3 **Small-signal transistors**

S4a **Low-frequency power transistors and hybrid modules**

S4b **High-voltage and switching power transistors**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Surface mounted semiconductors**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 **Power MOS transistors**

S10 **Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1 **Bipolar ICs for radio and audio equipment**

IC2 **Bipolar ICs for video equipment**

IC3 **ICs for digital systems in radio, audio and video equipment**

IC4 **Digital integrated circuits**
CMOS HE4000B family

IC5 **Digital integrated circuits – ECL**
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs

IC6 **Professional analogue integrated circuits**

IC7 **Signetics bipolar memories**

IC8 **Signetics analogue circuits**

IC9 **Signetics TTL logic**

IC10 **Signetics Integrated Fuse Logic (IFL)**

IC11 **Microprocessors, microcomputers and peripheral circuitry**

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	
IC03N	**Telephony equipment** Bipolar, MOS	
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**PC54/74HC/HCU/HCT logic families** HCMOS	
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	(published 1984)
IC09N	**Logic series** TTL	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Analogue - industrial**	
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom integrated fuse logic** IFL series 20/24/28	
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	
IC15N	**Logic series** FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1 **Assemblies for industrial use**
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Synchronous motors and gearboxes**

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Variable resistors and test switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Film capacitors, ceramic capacitors**

C16 **Permanent magnet materials**

C17 **Stepping motors and associated electronics**

C18 **D.C. motors**

C19 **Piezoelectric ceramics**

C20 **Wire-wound components**

NUMERICAL AND FUNCTIONAL INDEX

NUMERICAL INDEX ECL 10 000 FAMILY

NUMERICAL INDEX ECL 100 000 FAMILY

FUNCTIONAL INDEX ECL 10 000 FAMILY

(selection guide)

FUNCTIONAL INDEX ECL 100 000 FAMILY

(selection guide)

GENERAL

Definitions of symbols and terms

Maximum ratings

DEFINITIONS OF SYMBOLS AND TERMS

The symbols and terms used in the data sheets have been chosen to agree with the standards of the International Electrotechnical Commission. The relative values of the specified conditions and limits are referenced to an algebraic scale. The extremities of the scale are:

max. is the most positive value of a spread (value closest to positive infinity).
min. is the most negative value of a spread (value closest to negative infinity).

Currents

Positive-current is defined as conventional current flow into a device pin. Negative current is defined as conventional current flow out of a device pin.

I_{EE} Power supply current. The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} Input current HIGH. The current flowing into a device pin with the specified V_{IH} applied to the input. This value represents the worst case d.c. input load that a device presents to a driving element.

I_{IHmax} The most positive value of I_{IH}.

I_{IHmin} The most negative value of I_{IH}.

I_{IL} Input current LOW. The current flowing into a device pin with the specified V_{IL} applied to the input.

I_{ILmax} The most positive value of I_{IL}.

I_{ILmin} The most negative value of I_{IL}.

I_{CC} Power supply current drawn from the positive supply.

I_{CCH} Current drawn from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drawn from V_{CC} power supply with all inputs at logic LOW level.

I_{CBO} Leakage current from input transistor on ECL devices without pull-down resistors.

I_{OS} Output short circuit current.

Voltages

V_T	Termination voltage for external output resistors (usually $V_T = -2$ V).
V_{BB}	Bias voltage. The internally generated reference voltage and output threshold levels.
V_{CC}	Circuit ground. This is the most positive potential in an ECL system and it is used as the reference level for other voltages.
V_{EE}	Power supply voltage. It is the most negative potential in the system.
V_{IH}	Input voltage HIGH. The range of input voltages that represents a logic HIGH level in the system.
V_{IHmin}	The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.
V_{IHmax}	The most positive V_{IH}.
V_{IL}	Input voltage LOW. The range of input voltages that represents a logic LOW level in the system.
V_{ILmin}	The most negative V_{IL}.
V_{ILmax}	The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.
V_{OH}	Output voltage HIGH. The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the outputs.
V_{OHmin}	The most negative V_{OH} under the specified input and loading conditions.
V_{OHmax}	The most positive V_{OH} under the specified input and loading conditions.
V_{OHC}	The output HIGH corner point or guaranteed HIGH output voltage with the inputs set to their respective threshold levels.
V_{OL}	Output voltage LOW. The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.
V_{OLmax}	The most positive V_{OL} under the specified input and loading conditions.
V_{OLmin}	The most negative V_{OL} under the specified input and loading conditions.
V_{OLC}	The output LOW corner point or guaranteed LOW output voltage with the inputs set to their respective threshold levels.

AC switching parameters

t_h	Hold time. Minimum time which a signal must be present and remain static *after* an active transition of the control input to guarantee the recognition of the data.
t_s	Set-up time. Minimum time which a signal must be present and remain static *before* an active transition at the control input to guarantee the recognition of the data.
t_w	Pulse width. The time between 50% amplitude points on the leading and trailing edges of a pulse to ensure proper action.
t_{THL}	Fall time. The transition time between two specified reference points (20 and 80%) on a waveform which is changing from HIGH to LOW.
t_{TLH}	Rise time. The time between two specified reference points (20 and 80%) on a waveform which is changing from LOW to HIGH.

t_{PLH} Rise propagation delay time. The time between the 50% points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Fall propagation delay time. The time between the 50% points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

f_{max}/f_C Count frequency/Toggle frequency/Operating frequency. The maximum repetition rate at which clock pulses may be applied to a sequential circuit.

t_R Release time. The minimum time before the active transition of the timing pulse clock or enable that reset must be released.

READ mode (memories)

t_{ACS} Chip select access time.

t_{RCS} Chip select recovery time.

t_{AA} Address access time.

WRITE mode (memories)

t_W Minimum write pulse.

t_{WSD} Data in set-up time.

t_{WSA} Address set-up time.

t_{WHA} Address hold time.

t_{WSCS} Chip select set-up time.

t_{WHCS} Chip select hold time.

t_{WS} Write desable time.

t_{WR} Write recovery time.

Temperature

T_{stg}	Maximum temperature at which device may be stored without damages or performance degradation.
T_j	Junction temperature.
T_{amb}	Ambient temperature.
$R_{th\ j\text{-}a}$	Thermal resistance of an IC package, junction to ambient.
$R_{th\ j\text{-}c}$	Thermal resistance of an IC package, junction to case.
$R_{th\ c\text{-}a}$	Thermal resistance of an IC package, case to ambient.

Miscellaneous

L_{fpm}	Linear feet per minute.
P_D	Total d.c. power applied to a device, not including any power delivered from the device to a load.
R_L	Load resistor (usually 50 Ω).
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
P.U.T.	Pin under test.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

MAXIMUM RATINGS

The limit parameters, beyond which the life of the devices may be impaired, are given in Table 1. In addition Table 2 provides certain limits, which, if exceeded, will not damage the devices but could degrade the performance below those of the guaranteed specifications.

Table 1 Limits beyond which device-life may be impaired.

parameters	symbol	10K	100K	unit
Supply voltage	V_{EE}	−8 to 0	−7 to 0	V
Input voltage (d.c.) $V_{CC} = 0$	V_I	V_{EE} to 0		V
Output source current (d.c.)	I_O	50	55	mA
Storage temperature	T_{stg}	−55 to + 150	−55 to + 150	°C
Junction temperature				
ceramic package	$T_{j\ max}$	165	150	°C
plastic package	$T_{j\ max}$	150	–	°C

Note:

For the ceramic package $T_{j\ max}$ may be exceeded (< 250 °C) for short periods of time (< 240 hours) without significant reduction in device life time.

Table 2 Limits beyond which performance may be degraded.

parameters	symbol	10K	100K	unit
Operating ambient temperature with air-flow $> 2{,}5$ m/s	T_{amb}	−30 to + 85	0 to + 85	°C
Supply voltage (d.c.)	V_{EE}	−4,68 to −5,72	−4,2 to −5,7	V
Load resistance to $V_T = -2$ V	R_L	50	50	Ω

Specifications in data sheets are limited
for 10K series $V_{EE} = -5{,}2 \pm 0{,}01$ V
for 100K series $V_{EE} = -4{,}2$ to $-4{,}8$ V.

FAMILY SPECIFICATIONS (ECL10 000)

ECL10 000

These specifications cover the electrical characteristics of the ECL10 000 unless otherwise specified in the individual device data sheet.

RATINGS: see chapter "MAXIMUM RATINGS"

D.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −5,2 V

Each CX circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. Test values are given in the table and defined in the figure.

Test parameters

	temperature °C			unit
	−30	+ 25	+ 85	
V_{IHmax}	−890	−810	−700	mV
V_{IHmin}	−1205	−1105	−1035	mV
V_{ILmax}	−1500	−1475	−1440	mV
V_{ILmin}	−1890	−1850	−1825	mV

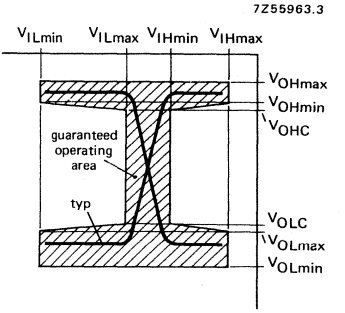


Fig. 1 Transfer characteristics.

A.C. CHARACTERISTICS

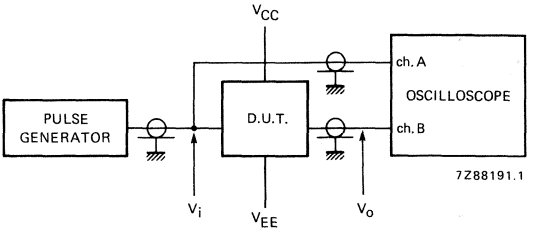


Fig. 2 Switching times test circuit. $V_{CC1} = V_{CC2}$ = + 2,0 V; V_{EE} = −3,2 V.

input pulse: $t_{TLH} = t_{THL}$ = 2,0 ± 0,2 ns (between 20 and 80%); V_{IH} = + 1,1 V; V_{IL} = + 0,3 V.

Test table V_{CC} = 0 V (ground); V_{EE} = −5,2 V; R_L = 50 Ω to −2 V.

characteristic	symbol	temperature (°C)			unit	remarks
		−30	+ 25	+ 85		
Output voltage HIGH	V_{OHmax}	−890	−810	−700	mV	
	V_{OHmin}	−1060	−960	−890	mV	
Output threshold voltage HIH	V_{OHC}	−1080	−980	−910	mV	
Output threshold voltage LOW	V_{OLC}	−1655	−1630	−1595	mV	
Output voltage LOW	V_{OLmax}	−1675	−1650	−1615	mV	
	V_{OLmin}	−1890	−1850	−1825	mV	

Notes

1. Input resistance is positive at any frequency.
2. Non-specified input pins should be connected to V_{ILmin} or left open.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal lenght.
4. Input impedance of the oscilloscope is 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper test.

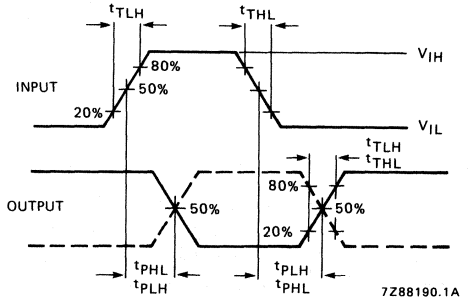


Fig. 3 Propagation delay and transition times waveforms

DEVICE DATA (ECL10 000)

QUADRUPLE 2-INPUT NOR GATE WITH STROBE

The 10100 is a quadruple 2-input NOR gate with another input common to all gates.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

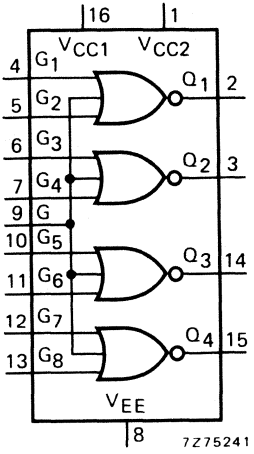


Fig. 1 Logic diagram.

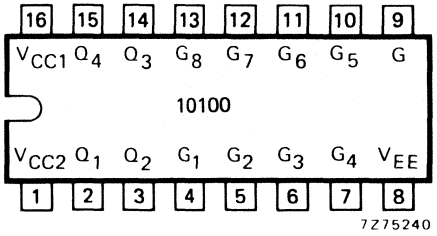


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground)
$V_{EE} = -5{,}2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5.2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}; t_{PHL}	typ.	2,0 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package outlines)

10100N: 16-lead DIL: plastic (SOT-38).
10100F: 16-lead DIL: ceramic (SOT-74)

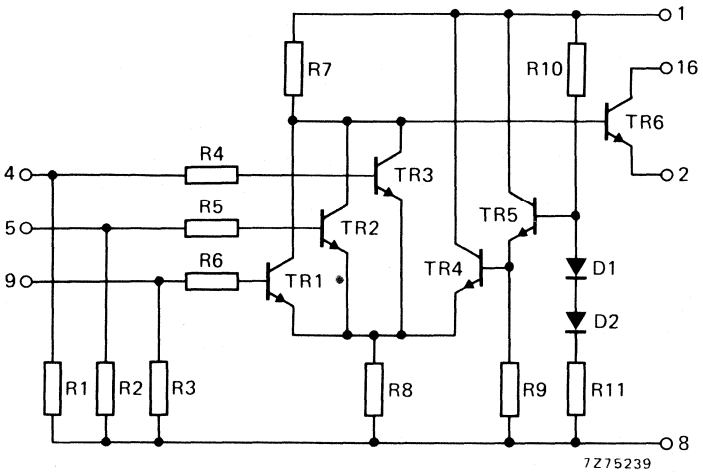
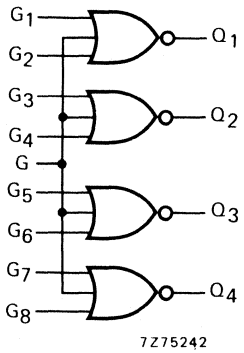


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G_2 + G}$

$Q_2 = \overline{G_3 + G_4 + G}$

$Q_3 = \overline{G_5 + G_6 + G}$

$Q_4 = \overline{G_7 + G_8 + G}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS: see chapter FAMILY SPECIFICATIONS

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2V

	symbol	pin under test	T_{amb} (°C)			unit	Conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	390	245	245	μA	
		9*	750	470	470	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	inputs at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	inputs at V_{IHmax}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min	−1 080	− 980	− 910	mV	one input at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{IHmax}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/t_{PHL}	min.	1,0	1,0	1,0	ns	50% to 50%
		typ.		2,0		ns	
		max.	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.		2,0		ns	
		max.	3,6	3,3	3,7	ns	

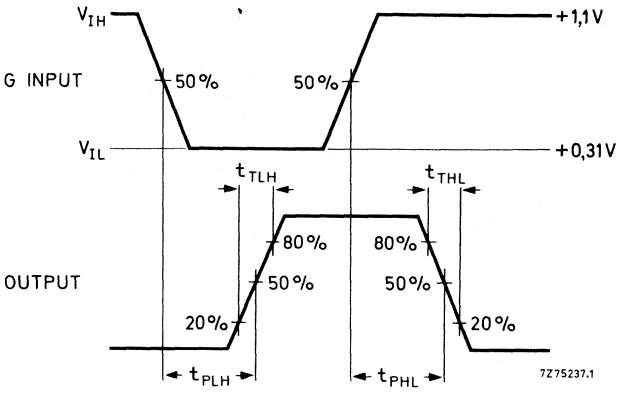


Fig. 5 Switching times testing waveforms.

QUADRUPLE OR/NOR GATE

The 10101 is a quadruple 2-input OR/NOR gate with one input from each gate common to pin 12.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

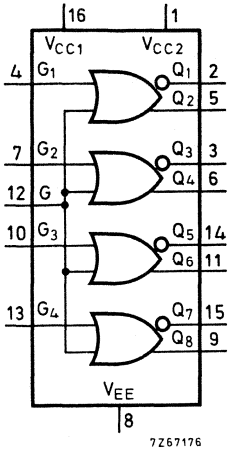


Fig. 1 Logic diagram.

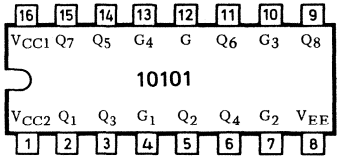


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5.2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no-load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package outlines)

10101N: plastic 16-lead dual in-line (SOT-38).
10101F: ceramic 16-lead dual in-line (SOT-74).

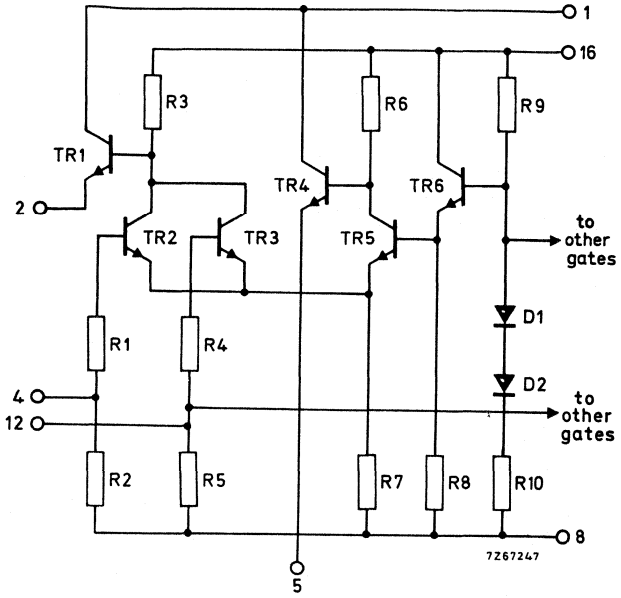
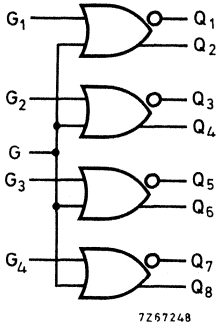


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G}$ $\quad Q_5 = \overline{G_3 + G}$

$Q_2 = G_1 + G$ $\quad Q_6 = G_3 + G$

$Q_3 = \overline{G_2 + G}$ $\quad Q_7 = \overline{G_4 + G}$

$Q_4 = G_2 + G$ $\quad Q_8 = G_4 + G$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	26	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	12*	850	535	265	μA	
		other inputs	425	265	265	μA	

* Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs for invert outputs
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	V_{IHmax} on inputs for direct outputs
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs for invert outputs
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin} on inputs for direct outputs
Output threshold voltage HIGH	V_{OHC}	min.	−1080	− 980	− 910	mV	V_{ILC} on one input for invert ouputs V_{IHC} on one input for direct outputs
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC} or V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	50% to 50%
		typ.		2,0		ns	
		max.	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80+
		typ.		2,0		ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE NOR GATE

The 10102 is a quadruple 2-input NOR gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply

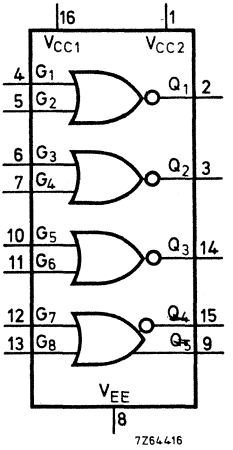


Fig. 1 Logic diagram.

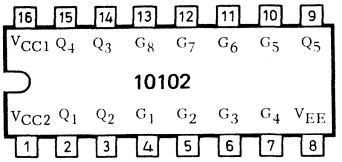


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10102N: plastic 16-lead dual in-line (SOT-38).
10102F: ceramic 16-lead dual in-line (SOT-74)

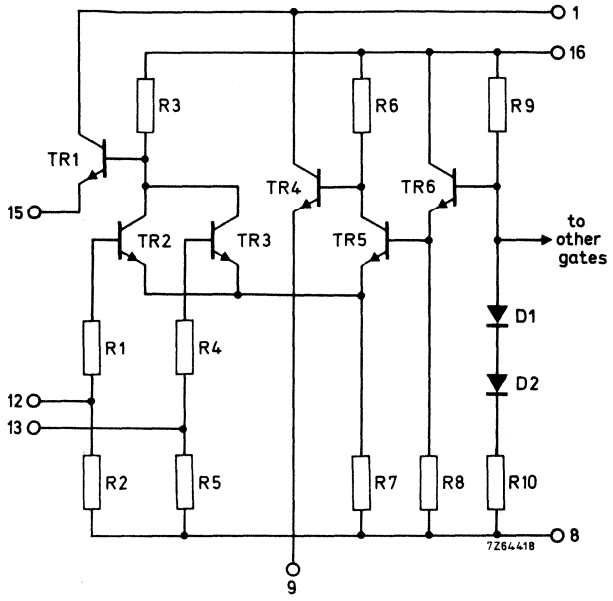
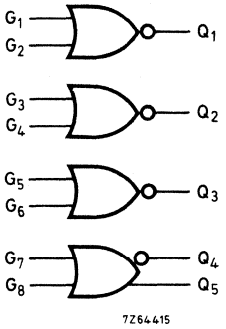


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1 + G_2}$
$Q_2 = \overline{G_3 + G_4}$
$Q_3 = \overline{G_5 + G_6}$
$Q_4 = \overline{G_7 + G_8}$
$Q_5 = \overline{Q_4}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	4 *	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the same above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs for invert outputs
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	V_{IHmax} on inputs 12;13 for output 9
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs for invert outputs
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin} on inputs 12;13 for output 9
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{ILC} on one input for invert outputs V_{IHC} on input 12 or 13 for input 9
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{ILC} or V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	50% to 50%
		max.	3,1	2,9	3,3	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-INPUT OR GATE

The 10103 is a quadruple 2-input 3 OR and 1 OR/NOR gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

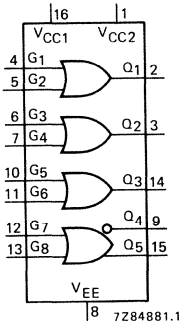


Fig. 1 Logic diagram.

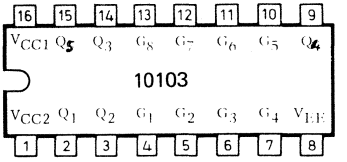


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10102N: plastic 16-lead dual in-line (SOT-38).
10102F: ceramic 16-lead dual in-line (SOT-74).

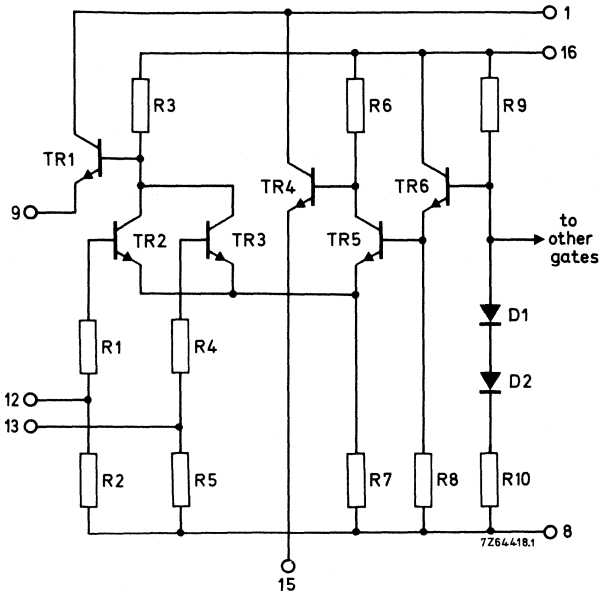
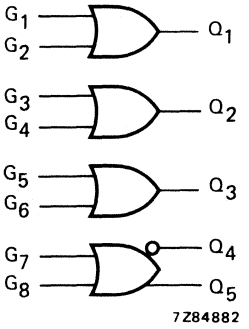


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 + G_2$
$Q_2 = G_3 + G_4$
$Q_3 = G_5 + G_6$
$Q_5 = G_7 + G_8$
$Q_4 = \overline{Q_5}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	390	245	245	μA	

*Individually test each input applying the same above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax} on inputs for direct output
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	V_{ILmin} on inputs for invert output
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin} on inputs for direct output
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax} on inputs for invert output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{ILC} on inputs for invert output V_{IHC} on inputs for direct output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on inputs for direct output V_{IHC} on inputs for invert output

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	50% to 50%
		max.	3,1	2,9	3,3	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-INPUT AND GATE

The 10104 is a high-speed logic, low power, AND function.
Open emitter outputs feature:
- easy choice of interface techniques.
- low power consumption when loaded by transmission lines.
- wired-OR capability of the outputs makes the device suitable for control, bussing and communications in high-speed processors, high-speed peripherals, instrumentation and digital communication systems.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

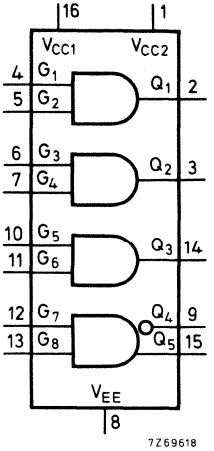


Fig. 1 Logic diagram.

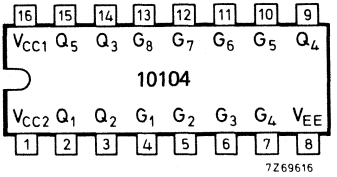


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2	V
Operating ambient temperature range	T_{amb}		−30 to + 85	°C
Average propagation delay	t_{PLH}	typ.	2,7	ns
Output voltage				
HIGH state	V_{OH}	nom.	−880	mV
LOW state	V_{OL}	nom.	−1720	mV
Power consumption per package (no load)	P_D	typ.	140	mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10104N: plastic 16-lead dual in-line (SOT-38).
10104F: ceramic 16-lead dual in-line (SOT-74).

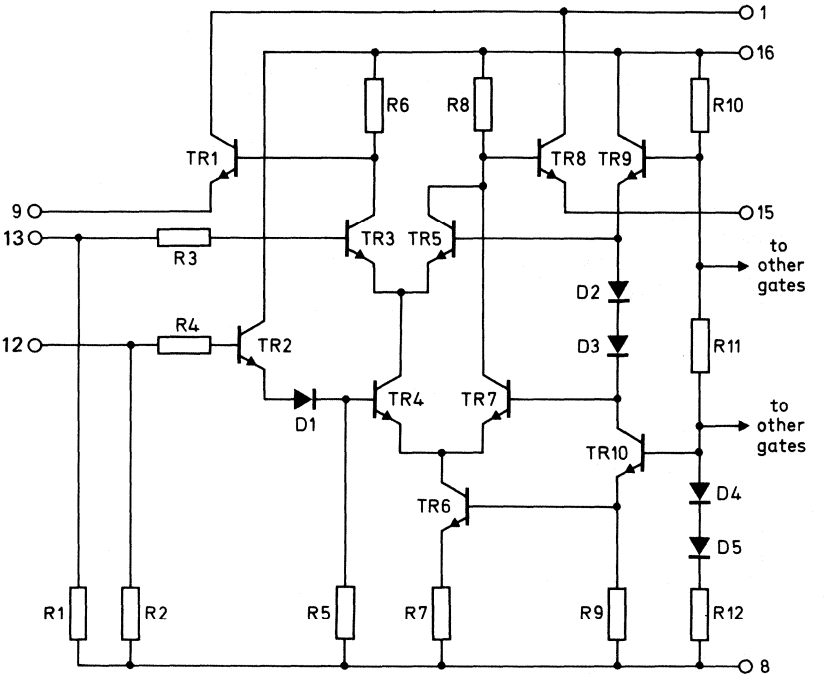
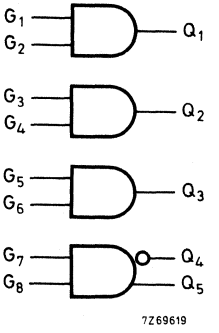


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 \cdot G_2$
$Q_2 = G_3 \cdot G_4$
$Q_3 = G_5 \cdot G_6$
$Q_4 = \overline{Q}_5$
$Q_5 = G_7 \cdot G_8$

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 4 Logic function.

RATINGS see chapter Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	39	35	39	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4,7,10,13	425	265	265	μA	
		5,6,11,12	350	220	220	μA	

*Individually test each input applying the same above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs for direct output
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	V_{IHmax} on inputs for invert output
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs for direct output
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin} on inputs for invert output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} on inputs for direct output; V_{ILC} on inputs for invert output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on inputs for direct output; V_{IHC} on inputs for invert output

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	50% to 50%
		typ.		2,7		ns	
		max.	4,3	4,0	4,2	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,7	3,5	3,6	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

TRIPLE OR/NOR GATE

The 10105 is a triple 2-3-2 input OR/NOR gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

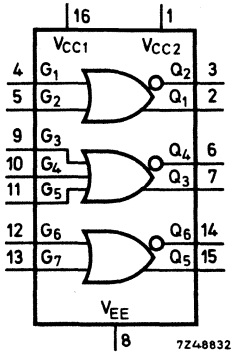


Fig. 1 Logic diagram.

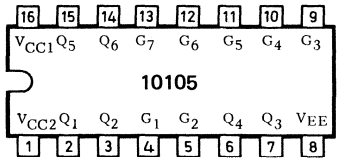


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{pd}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	75 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10105N: plastic 16-lead dual in-line (SOT-38).
10105F: ceramic 16-lead dual in-line (SOT-74).

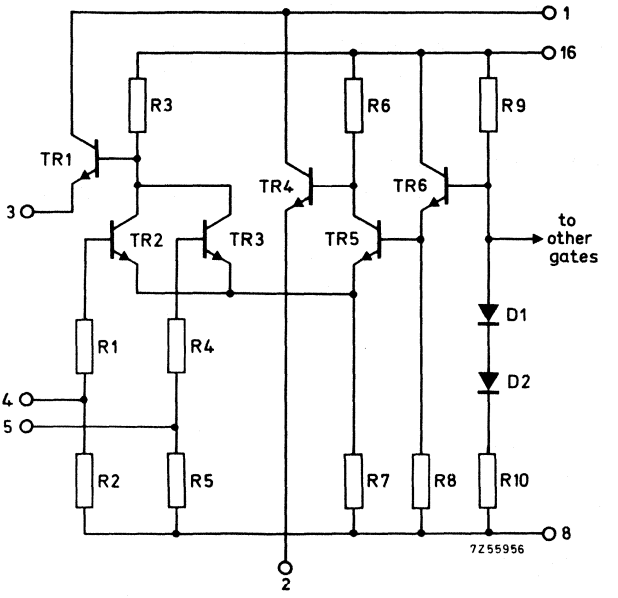
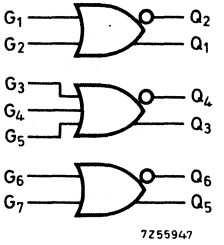


Fig. 3 Circuit diagram (one gate).



$Q_1 = G_1 + G_2$ $\quad Q_2 = \overline{G_1 + G_2}$

$Q_3 = G_3 + G_4 + G_5$ $\quad Q_4 = \overline{G_3 + G_4 + G_5}$

$Q_5 = G_6 + G_7$ $\quad Q_6 = \overline{G_6 + G_7}$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	23	21	23	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax}
		typ.		− 880		mV	or
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin}
		typ.		−1 720		mV	or
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC} or V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC} or V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	50% to 50%
		max.	3,1	2,9	3,3	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

TRIPLE NOR GATE

The 10106 is a triple 4-3-3 input NOR gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

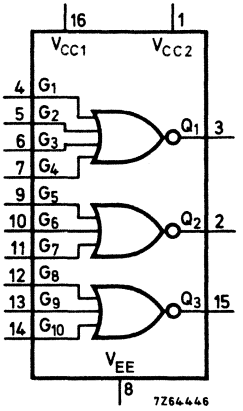
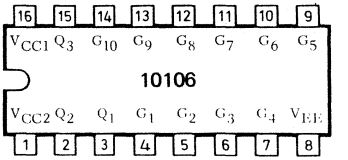


Fig. 1 Logic diagram.



Pin 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}/t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	75 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10106N: plastic 16-lead dual in-line (SOT-38).
10106F: ceramic 16-lead dual in-line (SOT-74).

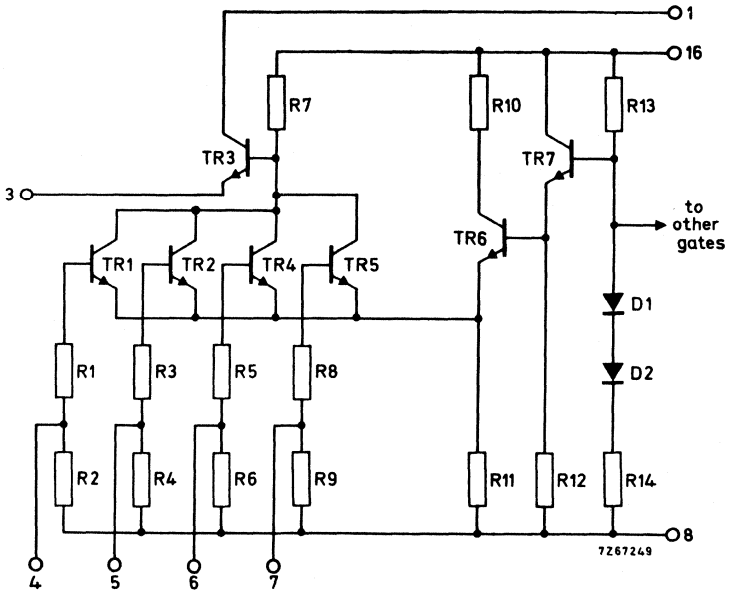
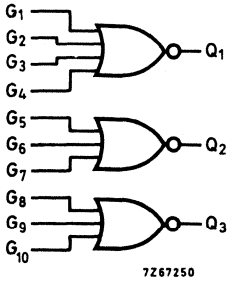


Fig. 3 Circuit diagram (one gate).



$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$
$$Q_2 = \overline{G_5 + G_6 + G_7}$$
$$Q_3 = \overline{G_8 + G_9 + G_{10}}$$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	23	21	23	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	one input at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	one input at V_{IHmax}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	one input at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	50% to 50%
		typ.		2,0		ns	
		max.	3,1	2,9	3,3	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.		2,0		ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

TRIPLE EXCLUSIVE OR/EXCLUSIVE NOR GATE

The 10107 is a three gate array designed to provide the positive EXCLUSIVE OR and NOR functions.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

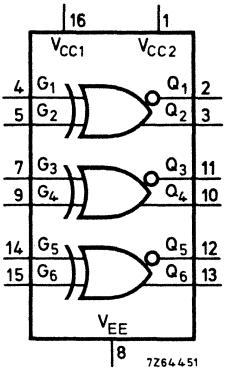


Fig. 1 Logic diagram.

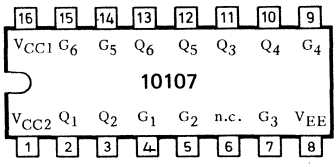


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,4 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	115 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINE (see Package Outlines)

10107N: plastic 16-lead dual in-line (SOT-38).
10107F: ceramic 16-lead dual in-line (SOT-74).

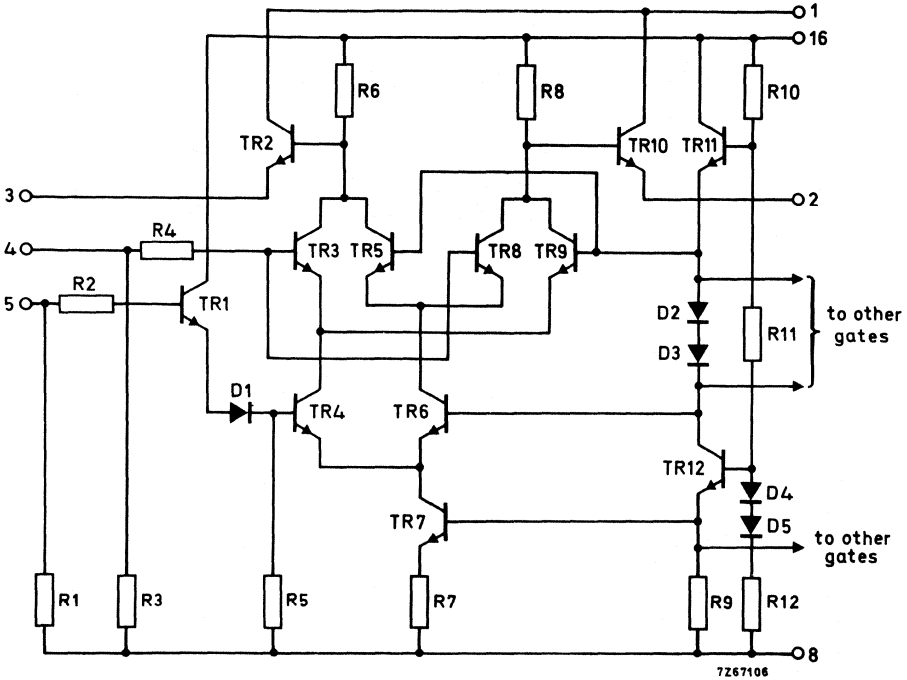
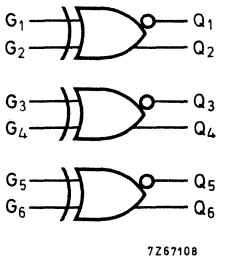


Fig. 3 Circuit diagram (one gate).



$Q_1 = \overline{G_1} \cdot \overline{G_2} + G_1 \cdot G_2$

$Q_2 = G_1 \cdot \overline{G_2} + \overline{G_1} \cdot G_2$

$Q_3 = \overline{G_3} \cdot \overline{G_4} + G_3 \cdot G_4$

$Q_4 = G_3 \cdot \overline{G_4} + \overline{G_3} \cdot G_4$

$Q_5 = \overline{G_5} \cdot \overline{G_6} + G_5 \cdot G_6$

$Q_6 = G_5 \cdot \overline{G_6} + \overline{G_5} \cdot G_6$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	31	28	31	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4,9,14	425	265	265	μA	
		5,7,15	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	
		typ.		− 880		mV	see note 1
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	
		typ.		−1 720		mV	see note 2
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	see note 3
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	see note 4

Notes:

1. V_{ILmin} or V_{IHmax} on both inputs for invert outputs.
   V_{ILmin} on one input and V_{IHmax} on other input for direct outputs.
2. V_{ILmin} on one input and V_{IHmax} on other input for invert outputs.
   V_{ILmin} or V_{IHmax} on both outputs for direct outputs.
3. V_{ILC} or V_{IHC} on both inputs for invert outputs.
   V_{ILC} on one input and V_{IHC} on other input for direct outputs.
4. V_{ILC} on one input and V_{IHC} on other input for invert outputs.
   V_{ILC} or V_{IHC} on both inputs for direct outputs.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,1	1,1	1,1	ns	
		typ.		2,4		ns	50% to 50%
		max.	3,8	3,7	4,0	ns	
transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,5		ns	20% to 80%
		max.	3,5	3,5	3,8	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

DUAL 4-INPUT AND/NAND GATE

The 10108 is a dual AND/NAND gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

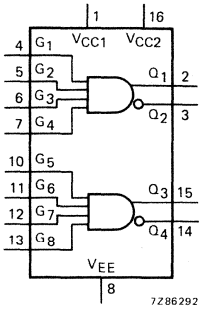


Fig. 1 Logic diagram.

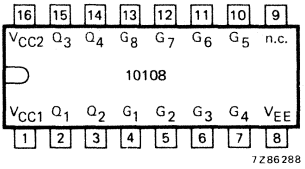


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}		−30 to + 85 °C
Average propagation delay			
AND output	t_{PLH}/t_{PHL}	typ.	2,3 ns
NAND output	t_{PLH}/t_{PHL}	typ.	2,8 ns
Power consumption per package (no load)	P_D	typ.	145 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10108N: plastic 16-lead dual in-line (SOT-38).
10108F: ceramic 16-lead dual in-line (SOT-74).

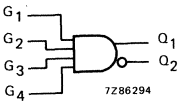


Fig. 3 Logic function
(one AND/NAND gate).

$Q_1 = G_1 \cdot G_2 \cdot G_3 \cdot G_4$

$Q_2 = \overline{Q}_1$

Positive logic
H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the more negative voltage) = 0

RATINGS see Family Specifications.

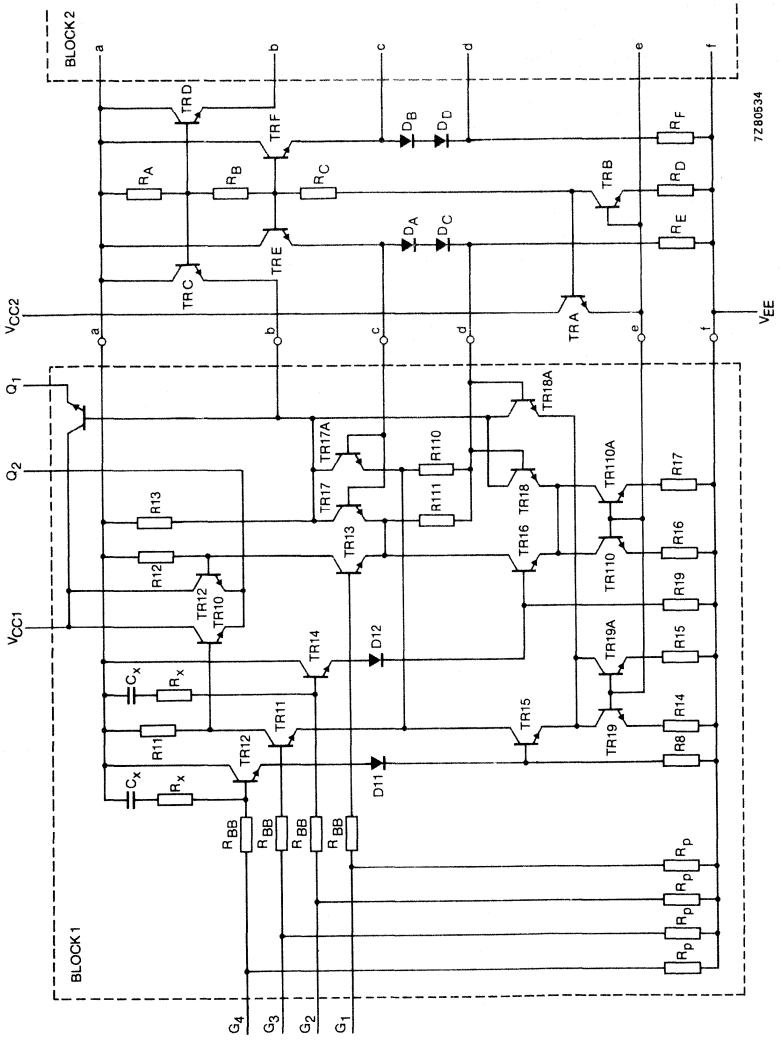


Fig. 4 Circuit diagram.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	40	36	40	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs for direct outputs
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	V_{IHmax} on inputs for invert output
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{IHmax} on inputs for direct output
		typ.		−1 720		mV	
		max.	−1.675	−1 650	−1 615	mV	V_{ILmin} on inputs for invert output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} on inputs for direct output; V_{ILC} on inputs for invert output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on inputs for direct output; V_{IHC} on inputs for invert output

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = − 3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,4	ns	50% to 50%
		typ.		2,3		ns	
		max.	4,1	3,7	4,1	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.		2,8		ns	
		max.	4,5	4,0	4,5	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

DUAL OR/NOR GATE

The 10109 is a dual 4-5 input OR/NOR gate.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

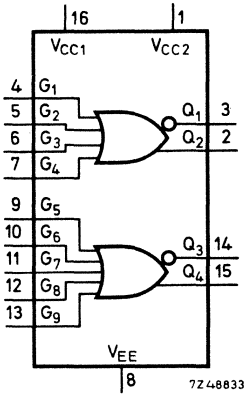


Fig. 1 Logic diagram.

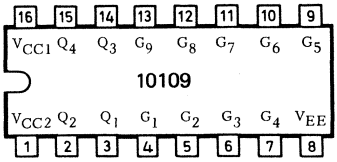


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	50 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines).

10109N: plastic 16-lead dual in-line (SOT-38).
10109F: ceramic 16-lead dual in-line (SOT-74).

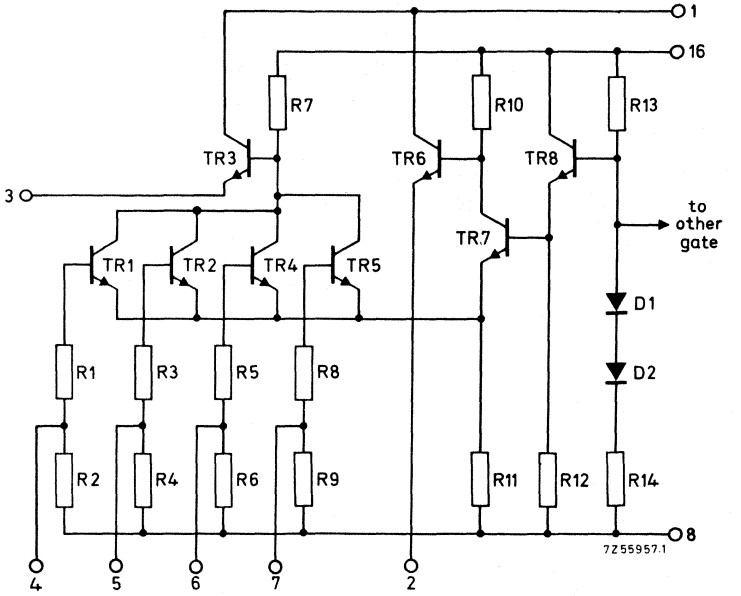
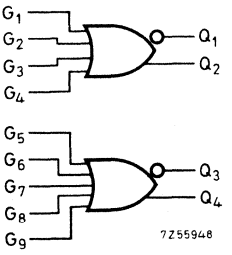


Fig. 3 Circuit diagram (one gate).



$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$

$$Q_3 = \overline{G_5 + G_6 + G_7 + G_8 + G_9}$$

$$Q_2 = G_1 + G_2 + G_3 + G_4$$

$$Q_4 = G_5 + G_6 + G_7 + G_8 + G_9$$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic functions.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	15	14	15	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4*	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax}
		typ.		− 880		mV	or
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin}
		typ.		−1 720		mV	or
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} or V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} or V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = − 3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	50% to 50%
		max.	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER

The 10110 is a dual 3-input/3-output OR gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

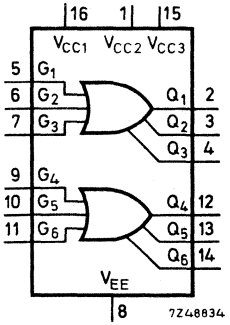


Fig. 1 Logic diagram.

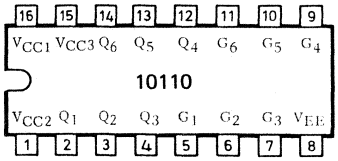


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay (all outputs loaded)	t_{PLH}	typ.	2,4 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	150 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10110N: plastic 16-lead dual in-line (SOT-38).
10110F: ceramic 16-lead dual in-line (SOT-74).

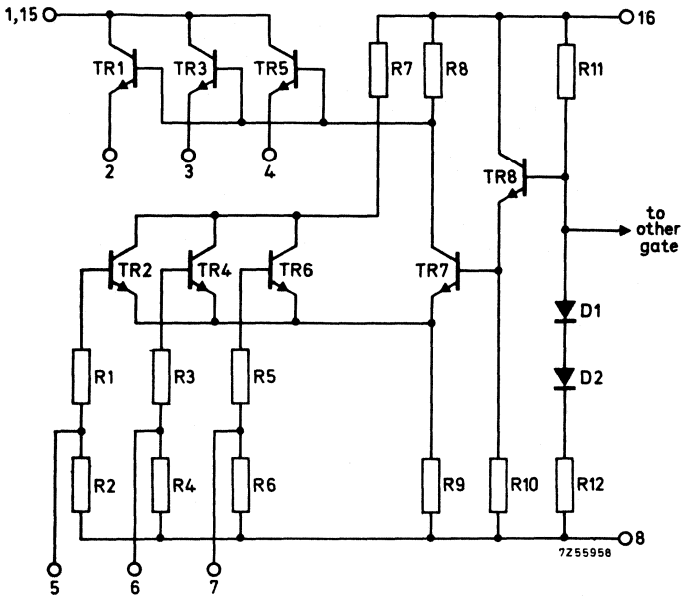
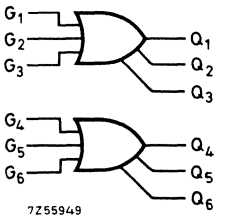


Fig. 3 Circuit diagram (one gate).



$Q_1 = Q_2 = Q_3 = G_1 + G_2 + G_3$

$Q_4 = Q_5 = Q_6 = G_4 + G_5 + G_6$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	42	38	42	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	5*	680	425	425	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	one input
		typ.		− 880		mV	at
		max.	− 890	− 810	− 700	mV	V_{IHmax}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	one input
		typ.		−1 720		mV	at
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	one input at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = − 3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,5	ns	all outputs
		typ.		2,4		ns	loaded
		max.	3,5	3,5	3,8	ns	50% to 50%
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,2	ns	all outputs
		typ.		2,2		ns	loaded
		max.	3,5	3,5	3,8	ns	20% to 80%

For **switching times test circuit** and **waveform** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT NOR LINE DRIVER

The 10111 is a dual 3-input/3-output NOR gate intended to drive up to three transmission lines simultaneously. The ability to control three parallel lines makes this device particularly useful in clock distribution applications.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

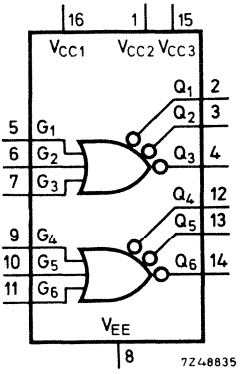


Fig. 1 Logic diagram.

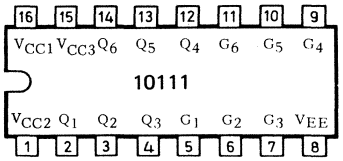


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay (all outputs loaded)	t_{PLH}	typ.	2,4 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	150 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10111N: plastic 16-lead dual in-line (SOT-38).
10111F: ceramic 16-lead dual in-line (SOT-74).

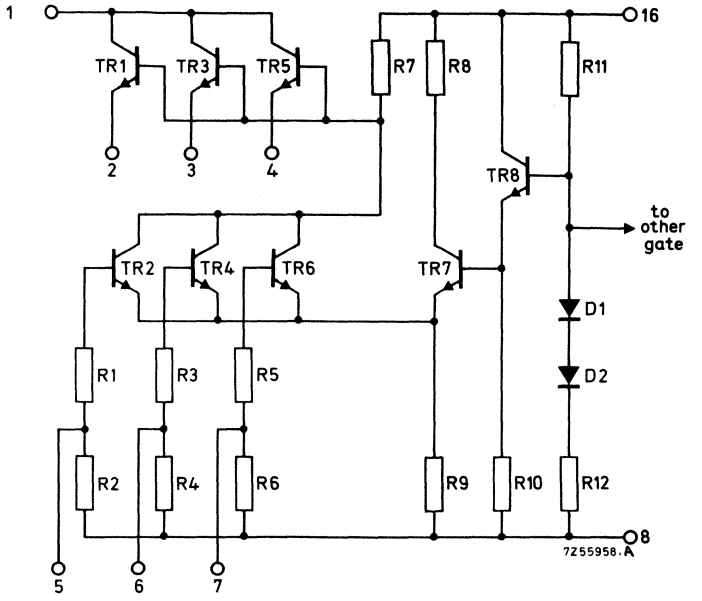


Fig. 3 Circuit diagram (one gate).

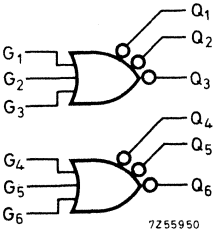


Fig. 4 Logic function.

$$Q_1 = Q_2 = Q_3 = \overline{G_1 + G_2 + G_3}$$
$$Q_4 = Q_5 = Q_6 = \overline{G_4 + G_5 + G_6}$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	42	38	42	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	5*	680	425	425	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	one input
		typ.		− 880		mV	at
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	one input
		typ.		−1 720		mV	at
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	one input at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = − 3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,5	ns	all outputs
		typ.		2,4		ns	loaded
		max.	3,5	3,5	3,8	ns	50% to 50%
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,2	ns	all outputs
		typ.		2,2		ns	loaded
		max.	3,5	3,5	3,8	ns	20% to 80%

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE EXCLUSIVE-OR GATE

The 10113 is a quadruple EXCLUSIVE-OR gate with an enable input common to all gates. The enable is active in LOW state. A 4-bit comparison function (A = B) can be obtained by wire-ORing the four outputs together. Direct connection to busses is possible thanks to open emitter outputs.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

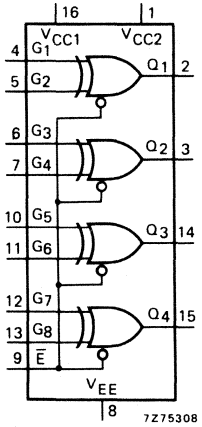


Fig. 1 Logic diagram.

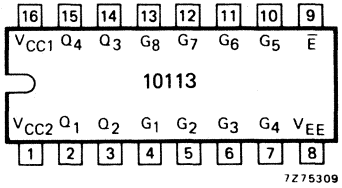


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	175 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10113N: plastic 16-lead dual in-line (SOT-38).
10113F: ceramic 16-lead dual in-line (SOT-74).

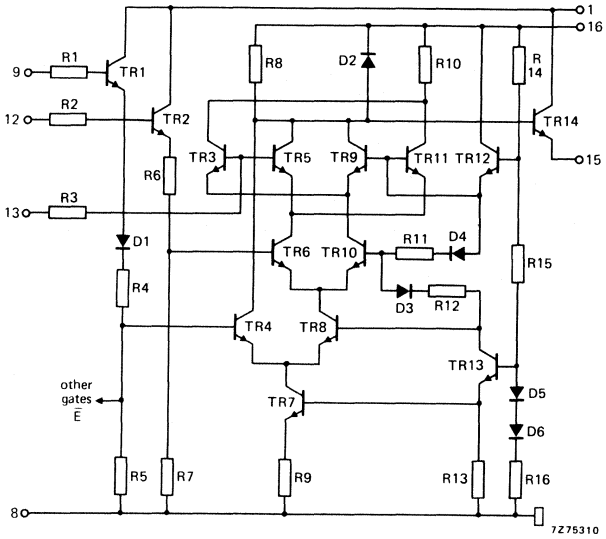


Fig. 3 Circuit diagram (one gate).

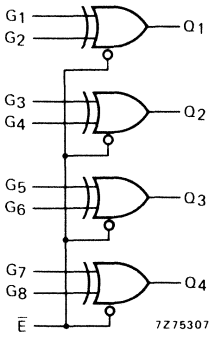


Fig. 4 Logic function.

$$Q_1 = \overline{G_1 + G_2 + \bar{E}}$$

$$Q_2 = \overline{G_3 + G_4 + \bar{E}}$$

$$Q_3 = \overline{G_5 + G_6 + \bar{E}}$$

$$Q_4 = \overline{G_7 + G_8 + \bar{E}}$$

FUNCTION TABLE

G_1	G_2	$\bar{E}$	Q_1
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
X	X	H	L

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	46	42	46	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4,7,10,13	425	265	265	μA	
		5,6,11,12	350	220	220	μA	
		9	870	545	545	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	one input at V_{IHmax}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	enable at V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	one output at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	enable at V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	one input at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	one input at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remark
			−30	+25	+85		
Rise propagation delay time	t_{PLH}	min.	1,1	1,3	1,3	ns	independent inputs
		max.	4,7	4,5	5,0	ns	
	t_{PLH}	min.	1,3	1,5	1,5	ns	enable input
		max.	5,2	5,0	5,5	ns	
Fall propagation delay time	t_{PHL}	min.	1,1	1,3	1,3	ns	independent inputs
		max.	4,7	4,5	5,0	ns	
	t_{PHL}	min.	1,3	1,5	1,5	ns	enable input
		max.	5,2	5,0	5,5	ns	
Rise time	t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	4,2	3,9	4,4	ns	
Fall time	t_{THL}	min.	1,1	1,1	1,1	ns	
		max.	4,2	3,9	4,4	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

TRIPLE LINE RECEIVER

The 10114 is a triple line receiver with low impedance emitter follower complementary outputs. With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ± 1 V. Furthermore, the OR outputs keep a LOW logic level, whenever the inputs are left floating. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high speed comparator and, having an internal reference supply voltage (V_{BB}), it can operate as a Schmitt trigger.

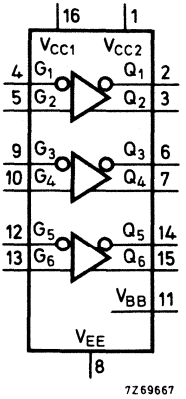


Fig. 1 Logic diagram

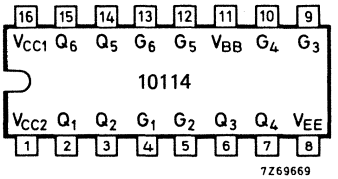


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		30 to +85 °C
Average propagation delay			
single-ended input	t_{PHL}	typ.	2,4 ns
differential input	t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	145 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10114N: plastic 16-lead dual in-line (SOT-38).
10114F: ceramic 16-lead dual in-line (SOT-74).

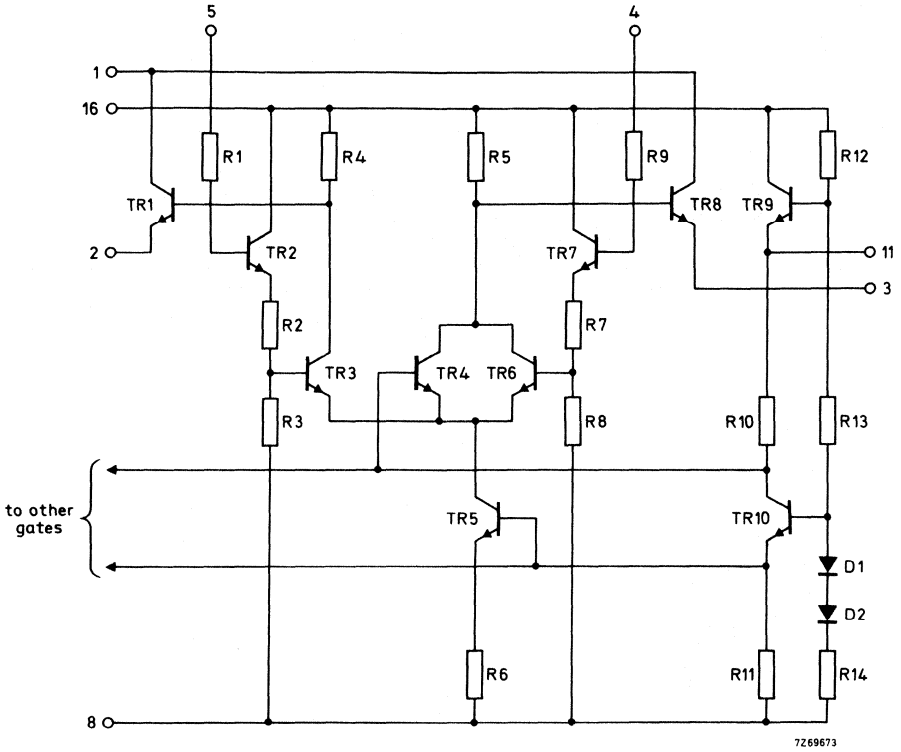


Fig. 3 Circuit diagram (one gate).

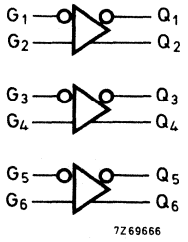


Fig. 4 Logic function.

With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)

$Q_1 = G_1$

$Q_2 = \overline{G_1}$

$Q_3 = G_3$

$Q_4 = \overline{G_3}$

$Q_5 = G_5$

$Q_6 = \overline{G_5}$

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	39	35	39	mA	for pins 4,9,12 $V_I = V_{ILmin}$ for pins 5,10,13 $V_I = V_{BB}$
Input current	I_{IHmax}	4*	70	45	45	μA	$V_I = V_{IHmax}$ see Fig. 5
	I_{CBOmax}	4 *	1,5	1,0	1,0	μA	test one input at a time $V_I = V_{EE}$ see Fig. 5
Reference voltage	min V_{BB}	11	−1 420	−1 350	−1 295	mV	see General spec "HOW TO TEST"
	max	11	−1 280	−1 230	−1 150	mV	

*Individually test each input applying the above mentioned conditions.

TEST PARAMETERS

To meet V_{OH} and V_{OL} specifications $V_I = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL} respectively to the other input of each gate.

symbol	T_{amb} (°C)			unit	remarks
	−30	+25	+85		
V_{IHH}	+ 110	+ 190	+ 300	mV	shifted +1 V
V_{IHmax}	− 890	− 810	− 700	mV	
V_{IHL}	−1 890	−1 810	−1 700	mV	shifted −1 V
V_{IHmin}	−1 205	−1 105	−1 035	mV	
V_{ILmax}	−1 500	−1 475	−1 440	mV	
V_{ILH}	− 890	− 850	− 825	mV	shifted + 1 V
V_{ILmin}	−1 890	−1 850	−1 825	mV	
V_{ILL}	−2 890	−2 850	−2 825	mV	shifted −1 V

V_{IHH} = V_{IHmax} shifted positive one volt for CMR tests.
V_{IHL} = V_{IHmax} shifted negative one volt for CMR tests.
V_{ILH} = V_{ILmin} shifted positive one volt for CMR tests.
V_{ILL} = V_{ILmin} shifted negative one volt for CMR tests.
(CMR: Common mode Rejection).

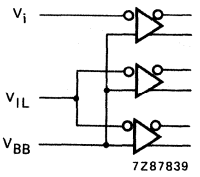


Fig. 5 Test circuit CMR test.

V_i = input under test.

V_{IL} input voltage shifted 1 Volt positive or negative.

	symbol	T_{amb} (°C)			unit	conditions
		−30	+25	+85		
Output voltage HIGH	min.	−1 060	− 960	− 890	mV	V_I at V_{IHmax}, invert output (1)
	V_{OH} typ.		− 880		mV	
	max.	− 890	− 810	− 700	mV	V_I at V_{ILmin}, direct output (1)
Output voltage LOW	min.	−1 890	−1 850	−1 825	mV	V_I at V_{ILmin}, invert output
	V_{OL} typ.		−1 720		mV	
	max.	−1 675	−1 650	−1 615	mV	V_I at V_{IHmax}, direct output (1)
Output threshold voltage HIGH	V_{OHCmin}.	−1 080	− 980	− 910	mV	V_I at V_{IHC}, invert output (1) / V_I at V_{ILC}, direct output (1)
Output threshold voltage low	V_{OLCmax}	−1 655	−1 630	−1 595	mV	V_I at V_{ILC}, invert output (1) / V_I at V_{IHC}, direct output (1)
Common mode rejection test	min. V_{OH}	−1 060	− 960	− 890	mV	V_{IHH} input 4, V_{ILH} input 5 for output 2
	max. V_{OH}	− 890	− 810	− 700	mV	V_{IHL} input 5, V_{ILL} input 4 for output 3
	min. V_{OL}	−1 890	−1 850	−1 825	mV	V_{IHL} input 5, V_{ILL} input 4 for output 2
	max. V_{OL}	−1 675	−1 650	−1 615	mV	V_{IHH} input 4, V_{ILH} input 5 for output 3

(1): See Fig. 5.

A.C. CHARACTERISTICS

V_{CC1} = VCC2 = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
propagation delay times	t_{PLH}/t_{PHL}	min.	1,0	1,0	0,9	ns	for single-ended input testing one input of each gate must be tied to V_{BB} (pin 11)
		typ.		2,4		ns	
		max.	4,4	4,0	4,3	ns	
transition times rise and fall	t_{TLH}/t_{THL}	min.	1,5	1,5	1,5	ns	20% to 80%
		max.	3,8	3,5	3,7	ns	

QUADRUPLE LINE RECEIVER

The 10115 is a quadruple differential amplifier intended for use in sensing signals over long lines. The base bias supply makes the device useful in other applications where a stable reference voltage is necessary.
With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ± 1V.

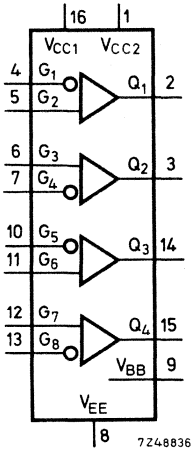


Fig. 1 Logic diagram.

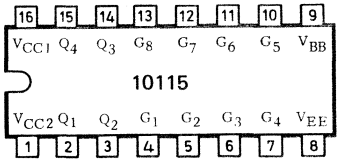


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	95 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10115N: plastic 16-lead dual in-line (SOT-38).
10115F: ceramic 16-lead dual in-line (SOT-74).

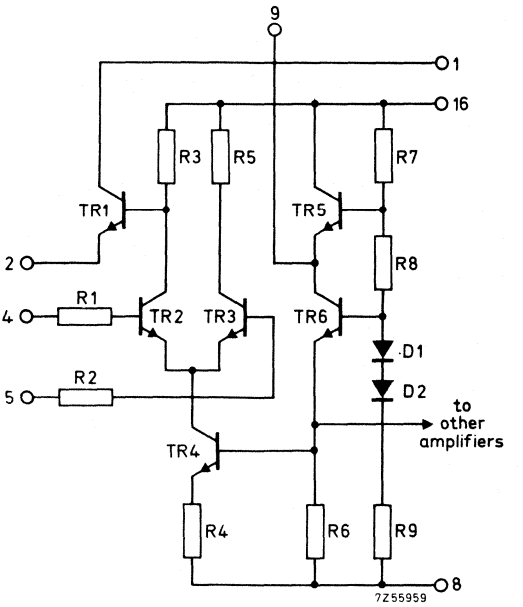


Fig. 3 Circuit diagram (one amplifier).

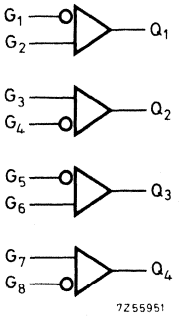


Fig. 4 Logic function.

With inputs G_2, G_3, G_6, G_7 connected to V_{BB}.

$Q_1 = \overline{G_1}$ $\quad Q_3 = \overline{G_5}$

$Q_2 = \overline{G_4}$ $\quad Q_4 = \overline{G_8}$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	pins 5,6,11,12 to V_{BB} pins 4,7,10,13 to V_{ILmin}
Input currents HIGH	I_{IHmax}	4*	150	95	95	μA	see Fig. 5 $V_I = V_{IHmax}$
	$ICBO_{max}$	4*	1,5	1,0	1,0	μA	see Fig. 5 $V_I = V_{EE}$
Reference voltage	V_{BB} min	9	−1 420	−1 350	−1 295	mV	see General spec "HOW TO TEST"
	V_{BB} max	9	−1 280	−1 230	−1 150	mV	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	for each gate: (1)
		typ.		− 880		mV	V_I at V_{ILmin}
		max.	− 890	− 810	− 700	mV	other input at V_{BB}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	for each gate: (1)
		typ.		−1 720		mV	V_I at V_{IHmax}
		max.	−1 675	−1 650	−1 615	mV	other input at V_{BB}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	for each gate: (1) V_I at V_{ILC} other input at V_{BB}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	for each gate: (1) V_I at V_{IHC} other input at V_{BB}

(1): See Fig. 5.

For common mode rejection test, use the same test configuration and limits as 10114 (Fig. 5).

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	for single-ended input testing one input of each gate must be tied to V_{BB} (pin 9)
		typ.		2,0		ns	
		max.	3,1	2,9	3,3	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.		2,0		ns	
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

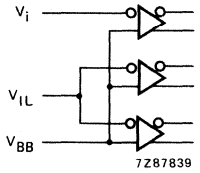


Fig. 5 Test circuit CMR test.

V_i = input under test.

V_{IL} input voltage shifted 1 Volt positive or negative.

TRIPLE LINE RECEIVER

The 10116 is a triple line receiver with low impedance emitter follower complementary outputs. With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ±1 V. Intended primarily to receive data from balanced twisted-pair lines, this device is also suitable for minicomputers, testing and instrumentation. It can also be used as a sense amplifier for MOS RAMs as a MOS-to-ECL interface circuit; as a high speed comparator and, having an internal reference supply voltage (V_{BB}), it can operate as a Schmitt trigger.

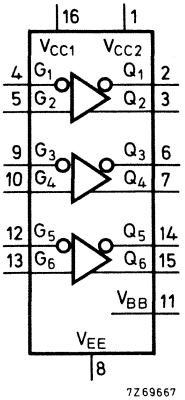


Fig. 1 Logic diagram.

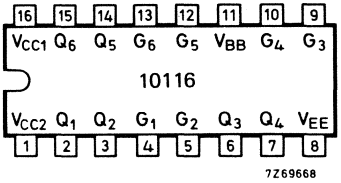


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = 5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay			
single-ended input	t_{PLH}	typ.	2,4 ns
differential input	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	85 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10116N: plastic 16-lead dual in-line (SOT-38).
10116F: ceramic 16-lead dual in-line (SOT-74).

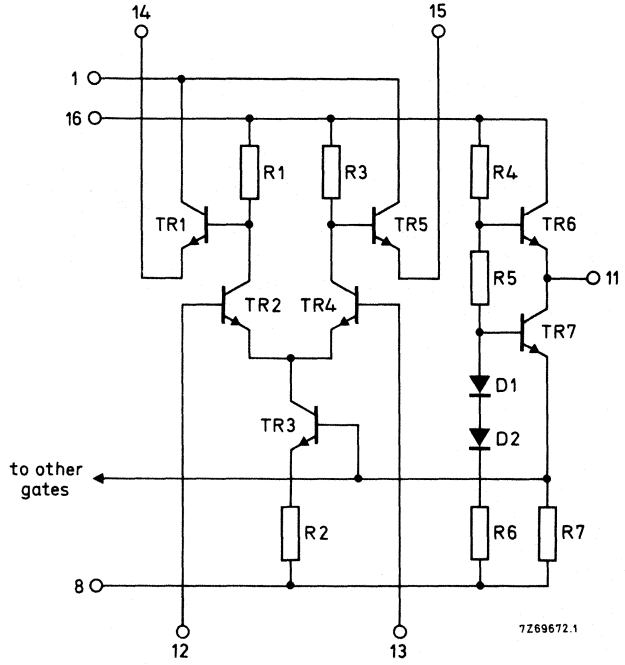


Fig. 3 Circuit diagram (one amplifier).

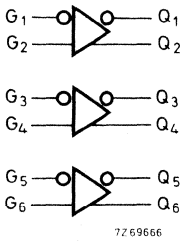


Fig. 4 Logic function.

With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)

$Q_1 = G_1$
$Q_2 = \overline{G}_1$
$Q_3 = G_3$
$Q_4 = \overline{G}_3$
$Q_5 = G_5$
$Q_6 = \overline{G}_5$

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	23	21	23	mA	pins 5,10,13 $V_I = V_{BB}$ pins 4,9,12 $V_I = V_{ILmin}$
Input currents HIGH	I_{IHmax}	4*	150	95	95	μA	see Fig. 5 $V_I = V_{EE}$
	I_{CBOmax}	4*	1,5	1,0	1,0	μA	see Fig. 5 $V_I = V_{EE}$
Reference voltage	V_{BB} min	11	−1 420	−1 350	−1 295	mV	see General spec "HOW TO TEST"
	V_{BB} max	11	−1 280	−1 230	−1 150	mV	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_I at V_{IH} max: (1)
		typ.		− 880		mV	invert output
		max.	− 890	− 810	− 700	mV	V_I at V_{ILmin} direct output
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_I at V_{ILmin}: (1)
		typ.		−1 720		mV	invert output
		max.	−1 675	−1 650	−1 615	mV	V_I at V_{IHmax} direct output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_I at V_{IHC}: (1) invert output V_I at V_{ILC} direct output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_I at V_{ILC}: (1) invert output V_I at V_{IHC} direct output

(1): See Fig. 5.

For common mode rejection test, use the same test configuration and limits as 10114 (Fig. 5).

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	for single-ended
		typ.		2,0		ns	input testing one
		max.	3,1	2,9	3,3	ns	input of each gate must be tied to V_{BB} (pin 11)
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

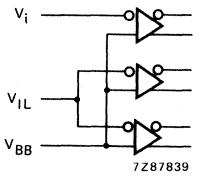


Fig. 5 Test circuit CMR test.

V_i = input under test.

V_{IL} input voltage shifted 1 Volt positive or negative.

DUAL OR-AND/OR-AND-INVERT GATE

The 10117 is a dual 2-wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

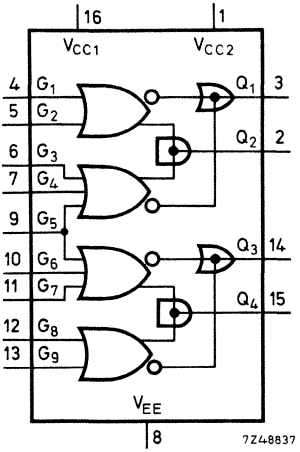


Fig. 1 Logic diagram.

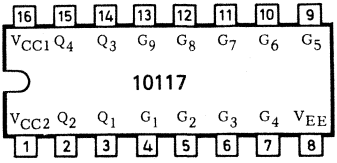


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines).

10117N: plastic 16-lead dual in-line (SOT-38).
10117F: ceramic 16-lead dual in-line (SOT-74).

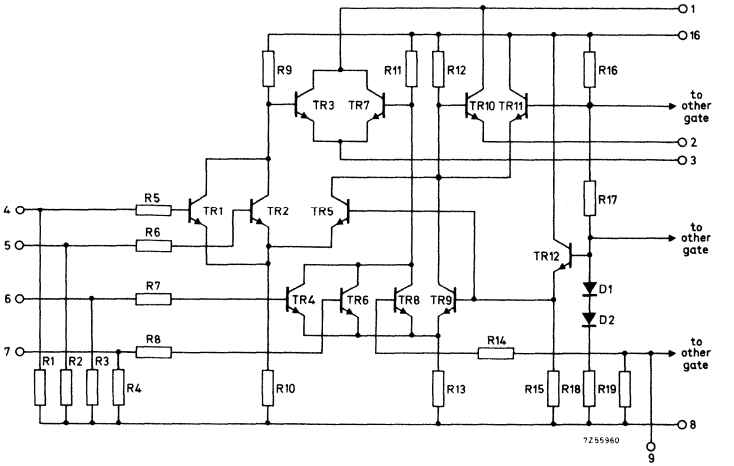


Fig. 3 Circuit diagram.

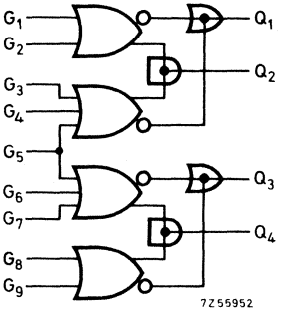


Fig. 4 Logic function.

$$Q_1 = \overline{(G_1 + G_2) \cdot (G_3 + G_4 + G_5)}$$
$$Q_2 = (G_1 + G_2) \cdot (G_3 + G_4 + G_5)$$
$$Q_3 = \overline{(G_8 + G_9) \cdot (G_5 + G_6 + G_7)}$$
$$Q_4 = (G_8 + G_9) \cdot (G_5 + G_6 + G_7)$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	26	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "HOW TO TEST SECTION"
Input current HIGH	I_{IHmax}	4,5,12,13	390	245	245	μA	
		6,7,10,11	425	265	265	μA	
		9	560	350	350	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax} or V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin} or V_{IHmax}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} or V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} or V_{IHC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,4	ns	
		typ.		2,3		ns	50% to 50%
		max.	3,9	2,4	3,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	0,9	1,1	1,1	ns	
		typ.		2,2		ns	20% to 80%
		max.	4,1	4,0	4,6	ns	

In order to enable the output, at least one input of the other gates wire-or'd to the gate under test must be high.

For **switching times test circuit** and **waveform** see Family Specifications.

DUAL OR-AND GATE

The 10118 is a dual 2-wide 3-input OR-AND gate designed for use in data control as a general purpose logic element.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

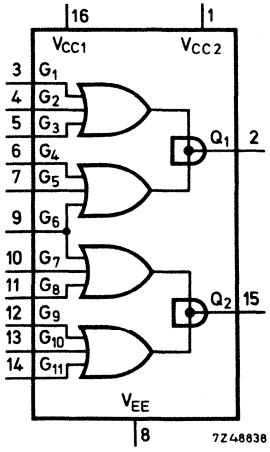


Fig. 1 Logic diagram.

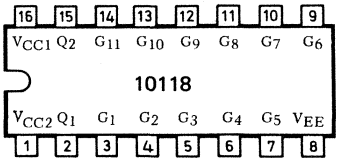


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH} typ.	2,3	ns
Output voltage			
HIGH state	V_{OH} nom.	−880	mV
LOW state	V_{OL} nom.	−1720	mV
Power consumption per package (no load)	P_D typ.	100	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines).

10118N: plastic 16-lead dual in-line (SOT-38).
10118F: ceramic 16-lead dual in-line (SOT-74).

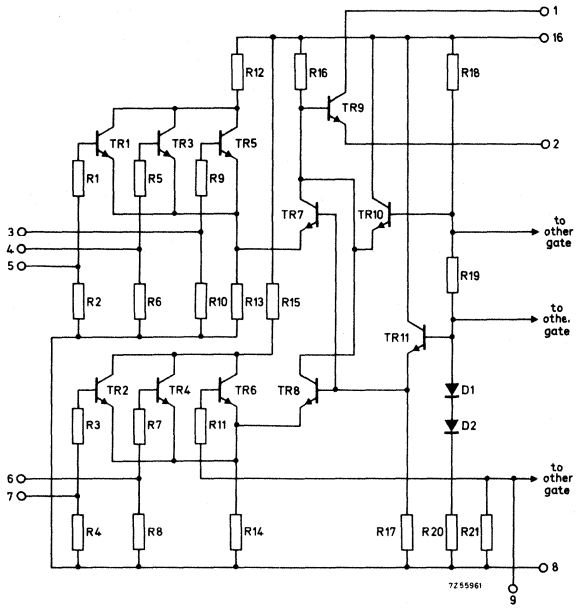


Fig. 3 Circuit diagram (one gate).

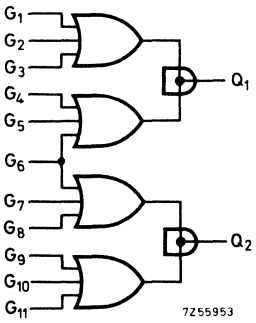


Fig. 4 Logic function.

$$Q_1 = (G_1 + G_2 + G_3) \cdot (G_4 + G_5 + G_6)$$
$$Q_2 = (G_6 + G_7 + G_8) \cdot (G_9 + G_{10} + G_{11})$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	3,4,5,12,13,14	390	245	245	μA	
		6,7,10,11	425	265	265	μA	
		9	560	350	350	μA	

*Individually test each input applying the above mentioned conditions

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	inputs at V_{IHmax}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−2 000	−1 990	−1 920	mV	inputs at V_{ILmin}
		typ.		−1 900		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	inputs at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	inputs at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,4	ns	50% to 50%
		typ.		2,3		ns	
		max.	3,9	3,4	3,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	0,8	1,1	1,1	ns	20% to 80%
		typ.		2,5		ns	
		max.	4,1	4,0	4,6	ns	

In order to enable the output, at least one input of the other gates wire-or'd to the gate under test must be high.

For **switching times test circuit** and **waveform** see Family Specifications.

OR-AND GATE

The 10119 is a 4-wide 4-3-3-3-input OR-AND gate designed for use in data control as a general purpose logic element.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

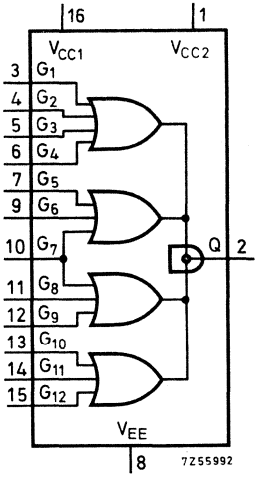


Fig. 1 Logic diagram.

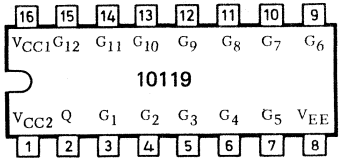


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10119N: plastic 16-lead dual in-line (SOT-38).
10119F: ceramic 16-lead dual in-line (SOT-74).

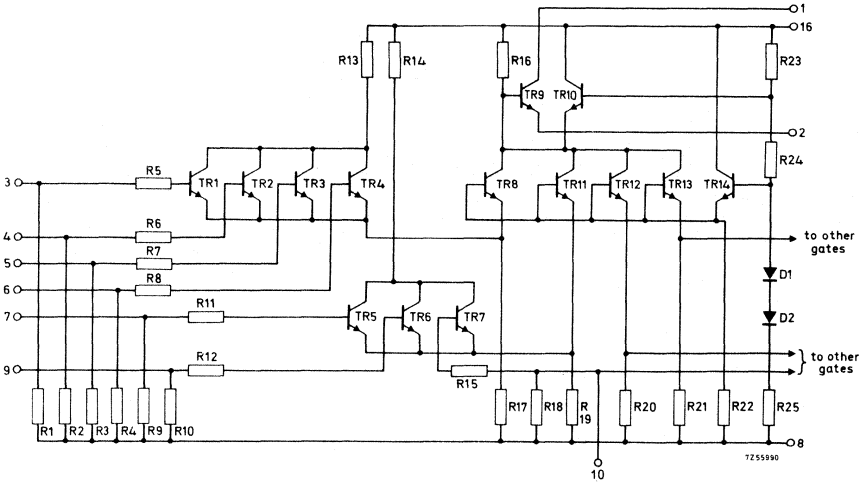


Fig. 3 Circuit diagram.

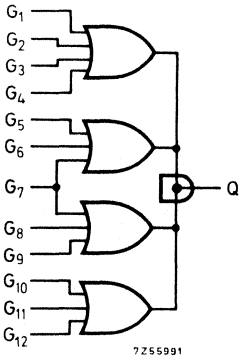


Fig. 4 Logic function.

$$Q = (G_1 + G_2 + G_3 + G_4) \cdot (G_5 + G_6 + G_7) \cdot (G_7 + G_8 + G_9) \cdot (G_{10} + G_{11} + G_{12}).$$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	3,4,5,12,13,14	390	245	245	μA	
		6,7,10,11	425	265	265	μA	
		9	560	350	350	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	inputs
		typ.		− 880		mV	at
		max.	− 890	− 810	− 700	mV	V_{IHmax}
Output voltage LOW	V_{OL}	min.	−2 000	−1 990	−1 920	mV	inputs
		typ.		−1 900		mV	at
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	inputs at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	inputs at V_{ILC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,4	1,4	1,4	ns	
		typ.		2,3		ns	50% to 50%
		max.	3,9	3,4	3,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	0,8	1,1	1,1	ns	
		typ.		2,5		ns	20% to 80%
		max.	4,1	4,0	4,6	ns	

In order to enable the output, at least one input of the other gates wire-or'd to the gate under test must be high.

For **switching times test circuit** and **waveform** see Family Specifications.

4-WIDE OR-AND/OR-AND-INVERT GATE

The 10121 is a 4-wide OR-AND/OR-AND-INVERT gate designed for use in data control as a general purpose logic element.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

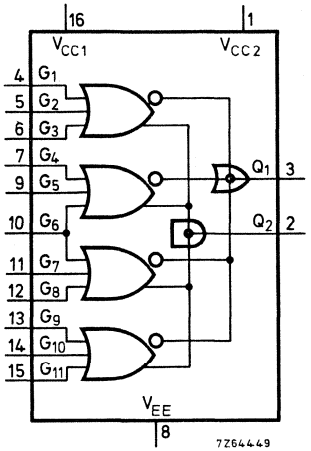


Fig. 1 Logic diagram.

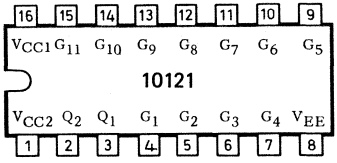


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	2,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mv
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D		100 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10121N: plastic 16-lead dual in-line (SOT-38).
10121F: ceramic 16-lead dual in-line (SOT-74).

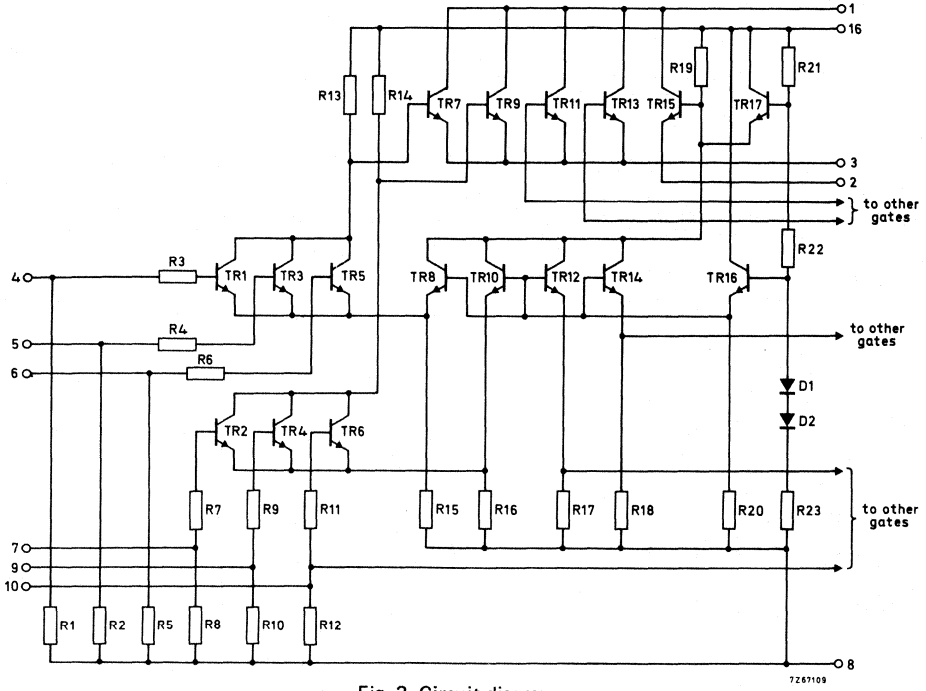
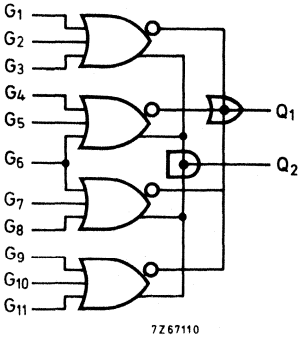


Fig. 3 Circuit diagram.



$$Q_1 = \overline{G_1 + G_2 + G_3} + \overline{G_4 + G_5 + G_6} + \overline{G_6 + G_7 + G_8} + \overline{G_9 + G_{10} + G_{11}}$$

$$Q_2 = \overline{Q_1}$$

positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	29	26	29	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	See "How to test Section"
Input current	I_{IHmax}	10	495	310	310	μA	
		other inputs	390	245	245	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{ILmin} on inputs for invert output
		typ.		− 880		mV	
		max.	− 780	− 700	− 590	mV	V_{IHmax} on inputs for direct output
Output voltage LOW	V_{OL}	min.	−2 000	−1 990	−1 920	mV	V_{ILmin} on inputs for direct output
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax} on inputs for invert output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{ILC} on inputs for invert output; V_{IHC} on inputs for direct output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on inputs for direct output; V_{IHC} on inputs for invert output

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min	1,4	1,4	1,4	ns	
		typ.		2,3		ns	50% to 50%
		max.	3,9	3,4	3,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	0,9	1,1	1,1	ns	
		typ.		2,5		ns	20% to 80%
		max.	4,1	4,0	4,6	ns	

In order to enable the output, at least one input of the gates wire-or'd to the gate under test must be high.

For **switching times test circuit** and **waveform** see Family Specifications.

TRIPLE NOR GATE

The 10123 consists of three NOR gates for use as a driver. It can drive a bus with a characteristic

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

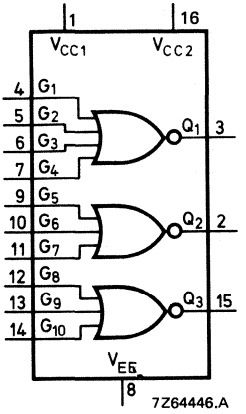


Fig. 1 Logic diagram.

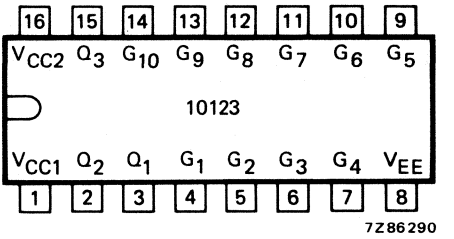


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0V$ (ground);
$V_{EE} = -5,2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}/t_{PHL}	typ. 3,0	ns
Power consumption per package (no load)	P_D	typ. 310	mW

FAMILY DATA
RATINGS } see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10123N: plastic 16-lead dual in-line (SOT-38).
10123F: ceramic 16-lead dual in-line (SOT-74).

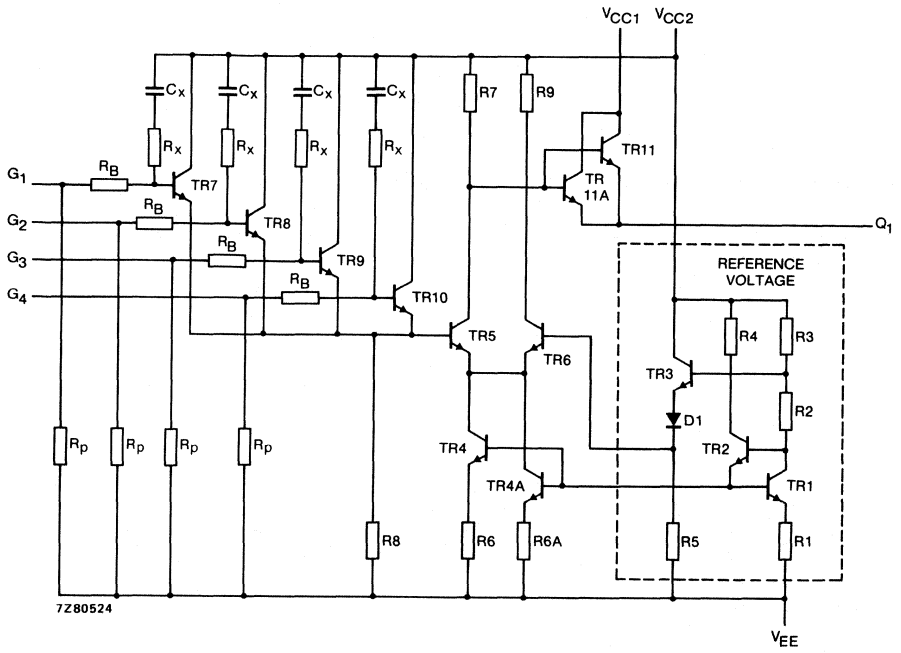


Fig. 3 Circuit diagram (one gate shown).

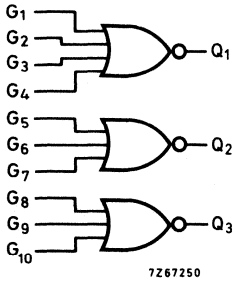


Fig. 4 Logic functions.

$$Q_1 = \overline{G_1 + G_2 + G_3 + G_4}$$

$$Q_2 = \overline{G_5 + G_6 + G_7}$$

$$Q_3 = \overline{G_8 + G_9 + G_{10}}$$

positive logic: HIGH state = 1
(the more positive voltage)
LOW state = 0
(the more negative voltage)

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	82	75	92	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	See "How to test Section"
Input current HIGH	I_{IHmax}	4*	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	R_L = 25 Ω to −2 V
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−2 100	−2 100	−2 100	mV	R_L = 25 Ω to −2.1 V
		max.	−2 030	−2 030	−2 030	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	R_L = 25 Ω to −2 V
Output threshold voltage LOW	V_{OLC}	max.	−2 010	−2 010	−2 010	mV	R_L = 25 Ω to −2.1 V

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min	1,2	1,2	1,2	ns	
		typ.		3,0		ns	50% to 50%
		max.	4,6	4,4	4,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,7	3,5	3,9	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

TTL-TO-ECL TRANSLATOR

The 10124 is a quadruple TTL-to-ECL translator with individual and common TTL-compatible inputs on each gate. When the common input is in the LOW state, all ECL direct outputs are in a LOW state and inverting outputs in a HIGH state.

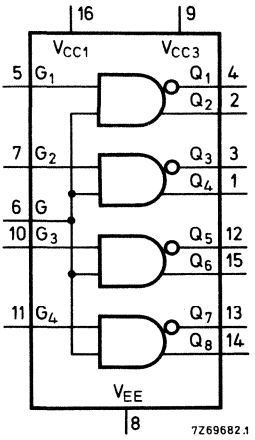


Fig. 1 Logic diagram.

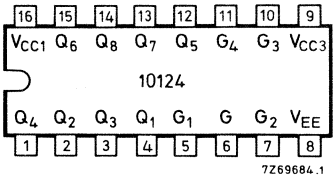


Fig. 2 Pin designation.

V_{CC1} = 0 V (ground);
V_{CC3} = +5 V;
V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 V
	V_{CC}		+5,0 V
	V_{CCmax}		+7,0 V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 3,5	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_D	typ. 380	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10124N: plastic 16-lead dual in-line (SOT-38).
10124F: ceramic 16-lead dual in-line (SOT-74).

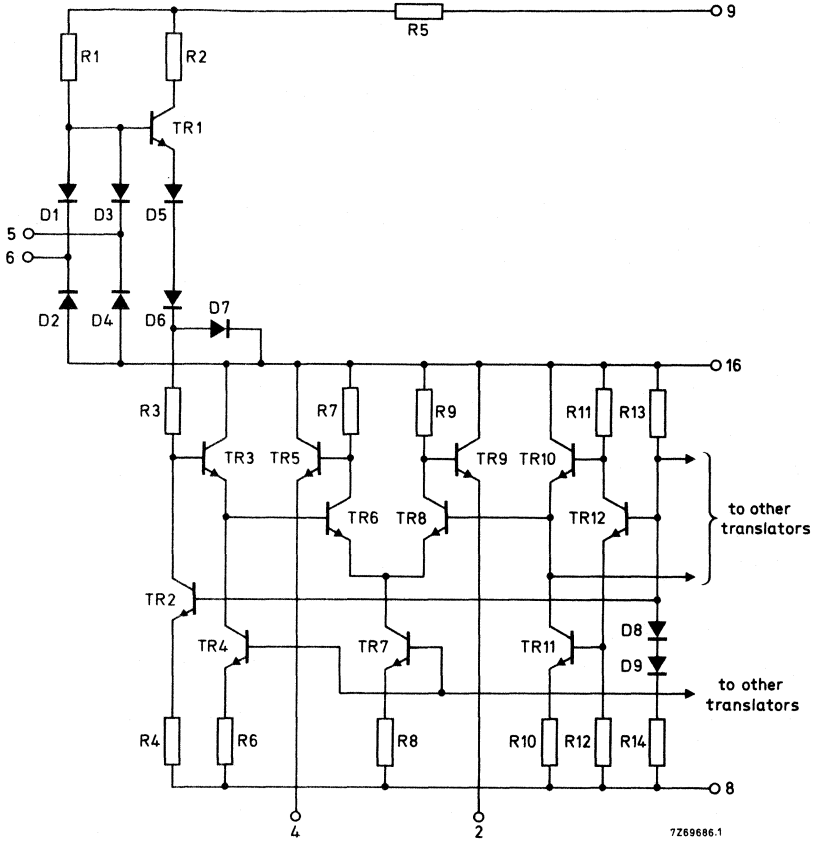


Fig. 3 Circuit diagram.

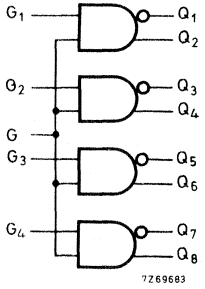


Fig. 4 Logic function.

$Q_1 = \overline{G_1 \cdot G}$ $\quad Q_5 = \overline{G_3 \cdot G}$

$Q_2 = G_1 \cdot G$ $\quad Q_6 = G_3 \cdot G$

$Q_3 = \overline{G_2 \cdot G}$ $\quad Q_7 = \overline{G_4 \cdot G}$

$Q_4 = G_2 \cdot G$ $\quad Q_8 = G_4 \cdot G$

Positive logic

H = HIGH state (the more positive voltage) = 1

L = LOW state (the less positive voltage) = 0.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC1} = ground; V_{CC3} =+5.0 V; V_{EE} = −5.2 V

	symbol	T_{amb} (°C)			unit	conditions
		−30	+25	+85		
Input voltage						
HIGH max	V_{IHmax}	4,0	4,0	4,0	V	
HIGH min	V_{IHmin}	2,0	1,8	1,8	V	
Input voltage						
LOW min	V_{ILmin}	0,4	0,4	0,4	V	
LOW max	V_{ILmax}	1,1	1,1	0,8	V	
Reverse voltage	V_R	2,4	2,4	2,4	V	
	V_{RH}	4,0	4,0	4,0	V	
Supply current	I_{EEmax}	72	66	72	mA	
	I_{CCHmax}	16	16	18	mA	$V_I = V_{RH}$ (all inputs)
	I_{CCLmax}	25	25	25	mA	
Reverse current						
Strobe input	I_{SR}	200	200	200	μA	$V_I = V_R$ (strobe) V_{ILmin} single inputs
single inputs	I_{IR}	50	50	50	μA	$V_I = V_{ILmin}$ (strobe) V_R (P.U.T.)
Forward current						
strobe input	I_{SF}	−12.8	−12.8	−12.8	mA	$V_I = V_{ILmin}$ (strobe) V_R (single inputs)
single inputs	I_{IF}	− 3.2	− 3.2	− 3.2	mA	$V_I = V_R$ (strobe) V_{ILmin} (P.U.T.)
Input breakdown voltage	$V_{I(BR)min}$	5,5	5,5	5,5	V	I_I strobe = 1 mA $V_I = V_{ILmin}$ while testing single inputs
Input clamping voltage						
I_5, I_7, I_{10}, I_{11}	$V_{I(CL)max}$	− 1,5	− 1,5	− 1,5	V	test one input at a time. I_I = −10 mA
I_6	$V_{I(CL)max}$	− 1,5	− 1,5	− 1,5	V	I_I = −20 mA

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Output voltage HIGH	V_{OH}	min.	−1 060	− 960	−890	mV	For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{IHmax} For outputs 3,4,12,13: pins 5,6,7,10,11 at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{ILmin} For outputs 1,2,14,15: pins 5,6,7,10,11 at V_{IHmax}
		typ		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For outputs 1,2,14,15: one input at V_{IHC} (1); other inputs at V_{IH} For outputs 3,4,12,13: one input at V_{ILC}; other inputs at V_{IH} (1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For outputs 1,2,14,15: one input at V_{ILC} (1); other inputs at V_{IHmax} For outputs 3,4,12,13: one input at V_{IHC}; other inputs at V_{IHmax}

V_{CC} must be applied before V_{EE} or simultaneously.

(1): per translator.

A.C. CHARACTERISTICS

V_{CC1} = 2.0 V; V_{CC3} = 7.0 V; V_{EE} = 3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	V_I (+1.5 V) to V_O (50%)
		typ.		3,5		ns	
		max.	6,8	6,0	6,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min	1,0	1,1	1,1	ns	20% to 80%
		max.	4,2	3,9	4,3	ns	

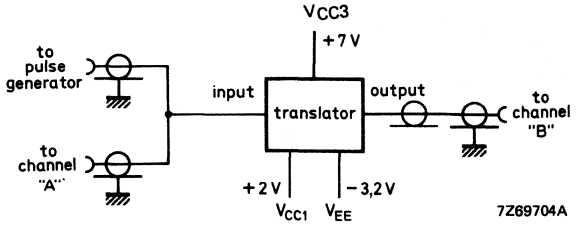


Fig. 5 Switching times test circuit.

Input pulse: $t_{TLH} = t_{THL} = 5{,}5$ ns (10 to 90%)

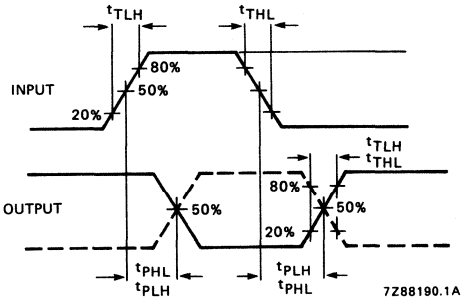


Fig. 6 Switching times waveforms. Input voltage at 50%1,5 V.

ECL-to-TTL TRANSLATOR

The 10125 is a quadruple ECL-toTTL translator for interfacing data between two different logic systems. It provides also a separate reference voltage (V_{BB}) to be used in case of single ended input biasing. Input and output levels are respectively ECL 10 000 and TTL Schottky.
With translated emitter follower inputs and an active current source, it features a common mode rejection peak voltage of ± 1V.

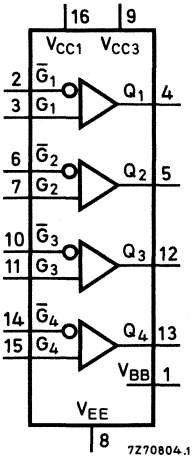


Fig. 1 Logic diagram.

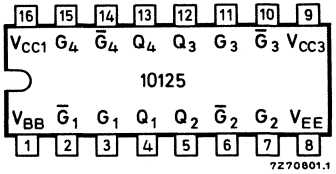


Fig. 2 Pin designation.

V_{CC1} = 0 V (ground);
V_{CC3} = +5 V;
V_{EE} = –5,2 V.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		–5,2 V
	V_{CC2}		+5,0 V
	V_{CCmax}		+7,0 V
Operating ambient temperature range	T_{amb}	–30 to + 85	°C
Average propagation delay	t_{PLH}	typ.	4,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	3,5 V
LOW state	V_{OL}	nom.	0,3 V
Power consumption per package (no load)	P_D	typ.	380 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10125N: plastic 16-lead dual in-line (SOT-38).
10125F: ceramic 16-lead dual in-line (SOT-74).

D.C. CHARACTERISTICS

V_{CCI} = 0 V (ground); V_{EE} = –5.2 V; V_{CC3} = +5 V

	symbol	Tamb (°C)			unit	conditions
		–30	+25	+85		
Supply current	I_{CCHmax}	52	52	52	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{IHmax}$
	I_{CCLmax}	39	39	39	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{ILmin}$
Supply current	I_{EEmax}	44	40	44	mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{ILmin}$
Input current	I_{IHmax}	180	115	115	μA	$V_{I1} = V_{IHmax}$ $V12 = V_{IHA}$ (Fig. 4)
	I_{CBOmax}	1,5	1,0	1,0	μA	$V_{I1} = V_{EE}$ $V_{12} = V_{EE}$ (Fig. 4)
Short-circuit output current	I_{OS} min I_{OS} max	40 100	40 100	40 100	mA mA	For pins 3,7,11,15 $V_I = V_{BB}$ For pins 2,6,10,14 $V_I = V_{ILmin}$ Connect outputs to ground, one at a time
Output voltage HIGH min	V_{OHmin}	2,5	2,5	2,5	V	Pins 2,6,10,14 $V_I = V_{ILmin}$ (1) Pins 3,7,11,15 $V_I = V_{IHmax}$
LOW max	V_{OLmax}	0,5	0,5	0,5	V	Pins 2,6,10,14 $V_I = V_{IHmax}$ Pins 3,7,11,15 (2) $V_I = V_{ILmin}$
Threshold voltage HIGH	V_{OHC}	2,5	2,5	2,5	V	Pins 2,6,10,14 $V_I = V_{ILmax}$ (one input a time) (1) Pins 3,7,11,15 $V_I = V_{BB}$
Threshold voltage LOW	V_{OLC}	0,5	0,5	0,5	V	Pins 2, 6, 10, 14 $V_I = V_{IHmin}$ (2) (one input at a time) Pins 3, 7, 11, 15 $V_I = V_{BB}$
Indeterminate input protection	$V_{OLSImax}$	0,5	0,5	0,5	V	All inputs at V_{EE} Test one gate at a time (2)
	$VOLS2max$	0,5	0,5	0,5	V	All inputs open (2)

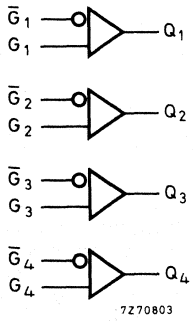
	symbol	T_{amb} (oC)			unit	conditions
		–30	+25	+85		
Reference voltage	V_{BB} min	–1 280	–1 230	–1 150	mV	See general specification "How we test"
	V_{BB} max	–1 420	–1 350	–1 295	mV	
Common mode rejection tests	V_{OHmin}	2,5	2,5	2,5	V	$V_I = V_{IHH}$ or V_{IHL} to one input of each gate under test (1) and $V_I = V_{ILH}$ or V_{ILL} respectively to the other input of each gate (2)
	V_{OLmax}	0,5	0,5	0,5	V	

(1) : Output current is –2.0 mA
(2) : Output current is +20.0 mA

A.C. CHARACTERISTICS

V_{CC1} = 0 (ground); V_{EE} = –5,2 V; V_{CC3} = 5,0 V

	symbol	pin under test	T_{amb} (oC)			unit	remarks
			–30	+25	+85		
Propagation delay times	t_{PLH}/t_{PHL}	min.	1,0	1,0	1,0	ns	Vi 50% to V_O = 1.5 V for single-ended input testing, one input from each gate must be tied to V_{BB} (pin 1)
		typ.		4,5		ns	
		max.	6,0	6,0	6,0	ns	
Transition times rise and fall	t_{TLH}/t_{THL}	max.	3,3	3,3	3,3	ns	(+1 V to +2 V)



$Q_1 = G_1$
$Q_2 = G_2$
$Q_3 = G_3$
$Q_4 = G_4$

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 3 Logic function.

TEST PARAMETERS

To meet V_{OH} and V_{OL} specifications $V_i = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL} respectively to the other input of each gate.

symbol	T_{amb} (°C)			unit	conditions
	–30	+25	+85		
V_{IHH}	+ 110	+ 190	+ 300	mV	shifted +1 V
V_{IHmax}	– 890	– 810	– 700	mV	
V_{IHL}	–1 890	–1 810	–1 700	mV	shifted –1 V
V_{IHmin}	–1 205	–1 105	–1 035	mV	
V_{ILmax}	–1 500	–1 475	–1 440	mV	
V_{ILH}	– 890	– 850	– 825	mV	shifted +1 V
V_{ILmin}	–1 890	–1 850	–1 825	mV	
V_{ILL}	–2 890	–2 850	–2 825	mV	shifted –1 V

$V_{IHH} = V_{IHmax}$ shifted positive one volt for CMR tests. (*)
$V_{IHL} = V_{IHmax}$ shifted negative one volt for CMR tests. (*)
$V_{ILH} = V_{ILmin}$ shifted positive one volt for CMR tests. (*)
$V_{ILL} = V_{ILmin}$ shifted negative one volt for CMR tests. (*)

(*): CMR = Common Mode Rejection.

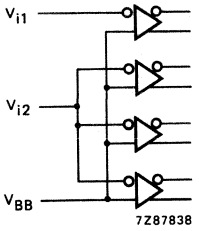


Fig. 4. Input current test circuit.
for I_{IH} $V_{i1} = V_{i2} = V_{IH}$ max.
for I_{CBO} $V_{i1} = V_{i2} = V_{EE}$

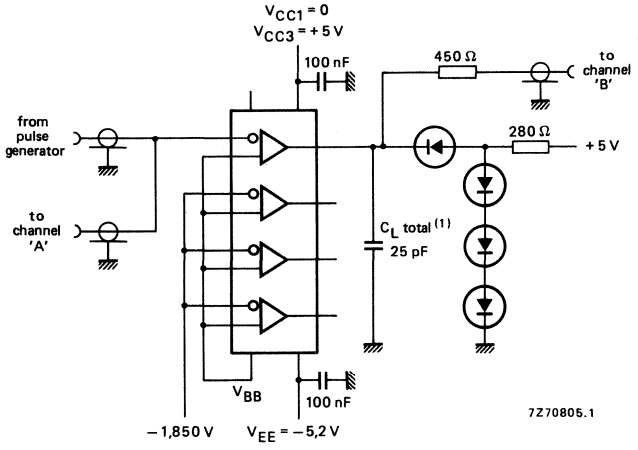


Fig. 5 Switching times test circuit

(1) including jig and stray capacitance

Input pulse: $t_{THL} = t_{TLH} = 2$ ns (20 to 80%)

One input from each gate must be tied to V_{BB} (Sin 1) during testing.

QUADRUPLE TTL/IBM BUS RECEIVER/LATCH

The 10129, is intended to allow interfacing of 10K family types with other logic devices or systems. All inputs, data, clock reset and strobe, are compatible with 10K family logic levels whereas data inputs accept TTL logic levels and levels compatible with IBM-type busses. The information received from the bus is stored temporarily in latch storage elements.

The strobe input is useful to provide accurate synchronization of signals and/or connection to 10K family type level busses. When the clock is LOW, the reset input is disabled and the inputs will follow the data inputs. The latches are capable of storing the data on the rising edge of the clock. Unused data inputs must be tied to V_{CC2} or ground. On the other hand, clock, strobe and reset inputs must be tied to V_{IL} or V_{EE} if unused.

The outputs are enabled when the strobe input is HIGH. Two modes of operation are provided. In the first mode, obtained by tying the hysteresis control input to V_{EE}, the input threshold points of the D inputs are fixed. In the second mode this hysteresis control input is connected to ground which gives an hysteresis input effect (see test table) useful for increasing the D input noise margin.

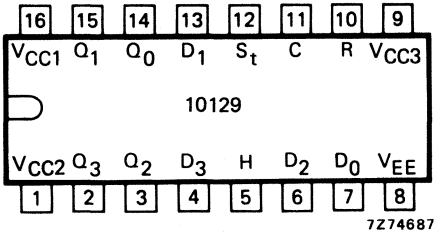


Fig. 1 Pin designation.

QUICK REFERENCE DATA

Supply voltages	V_{EE}		−5,2 V
	V_{CC3}		+5,0 V
	V_{CCmax}		+7,0 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	10 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
Output voltage LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	750 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10129N: plastic 16-lead dual in-line (SOT-38).
10129F: ceramic 16-lead dual in-line (SOT-74).

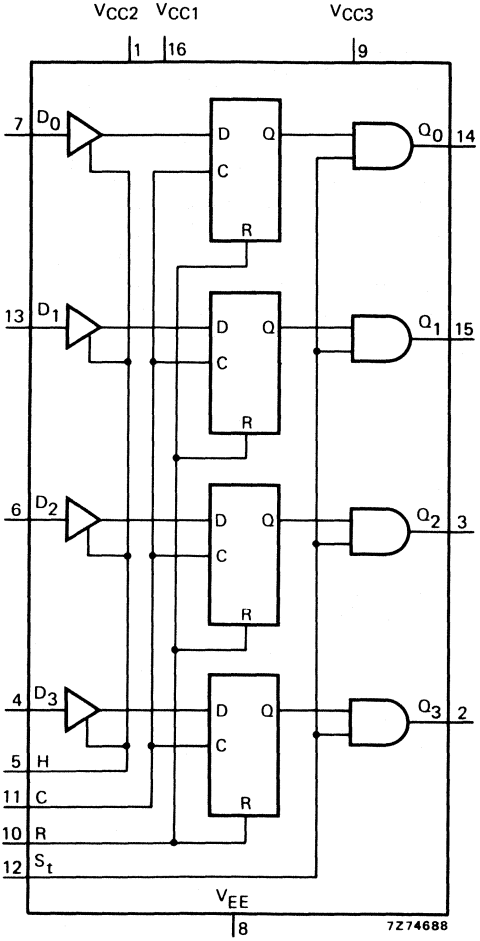


Fig. 2 Logic diagram.

D_0 to D_3	data inputs
H	hysteresis control
C	clock input
R	reset
S_t	strobe input
Q_0 to Q_3	outputs

inputs				output
D_n	C	S_t	R	$Q_n + 1$
X	X	L	X	L
X	H	X	H	L
L	L	H	X	L
X	H	H	L	Q_n
H	L	H	X	H

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

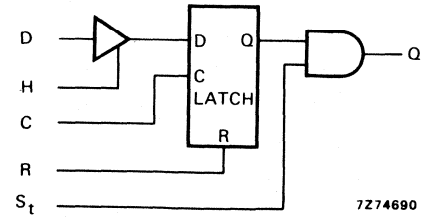


Fig. 3 Function table (one latch).

RATINGS see Family Sepcifications

TEST PARAMETERS

TTL Input levels

symbol	T_{amb} (°C)			unit
	–30	+25	+85	
V_{IHA}	3,000	3,000	3,000	V
V_{IHB}	2,000	2,000	2,000	V
V_{ILA}	0,800	0,800	0,800	V
V_{ILB}	0,400	0,400	0,400	V

IBM Input levels

symbol	T_{amb} (°C)			unit
	–30	+25	+85	
V_{IHA}	3,11	3,110	3,11	V
V_{IHB}		1,700		V
V_{ILA}		1,100		V
V_{ILB}	0,15	0,150	0,15	V

Hysteresis mode threshold voltages

symbol	T_{amb} (°C)			unit	remarks
	–30	+25	+85		
V_{IHA}''	2,900	2,600	2,300	V	L → H
V_{ILA}''	2,000	1,700	1,400	V	
V_{IHA}'''	2,200	1,900	1,600	V	H → L
V_{ILA}'''	1,300	1,000	0,700	V	

V_{IHA}'', V_{ILA}'', V_{IHA}''' and V_{ILA}''' are logic. "1" and "0" threshold voltages in the hysteresis mode as shown in Fig. 4.

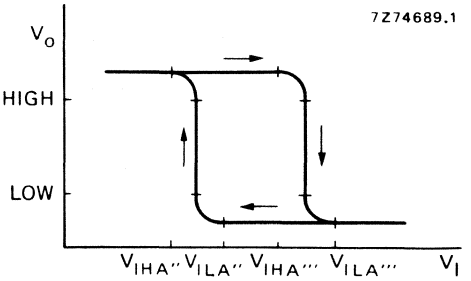


Fig. 4 Hysteresis mode threshold voltage.

ECL Input levels

symbol	T_{amb} (°C)			unit
	–35	+25	+85	
V_{IHmax}	– 890	– 810	– 700	mV
V_{IHmin}	–1 205	–1 105	–1 035	mV
V_{ILmax}	–1 500	–1 475	–1 440	mV
V_{ILmin}	–1 890	–1 850	–1 825	mV

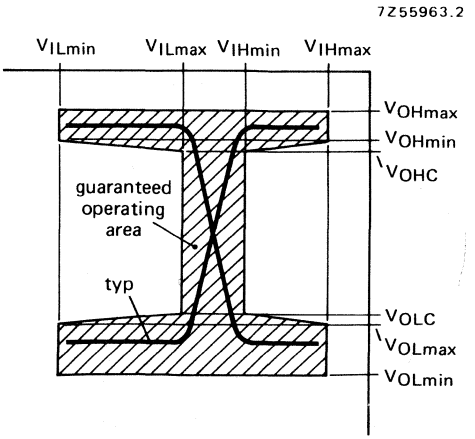


Fig. 5 Transfer characteristics.

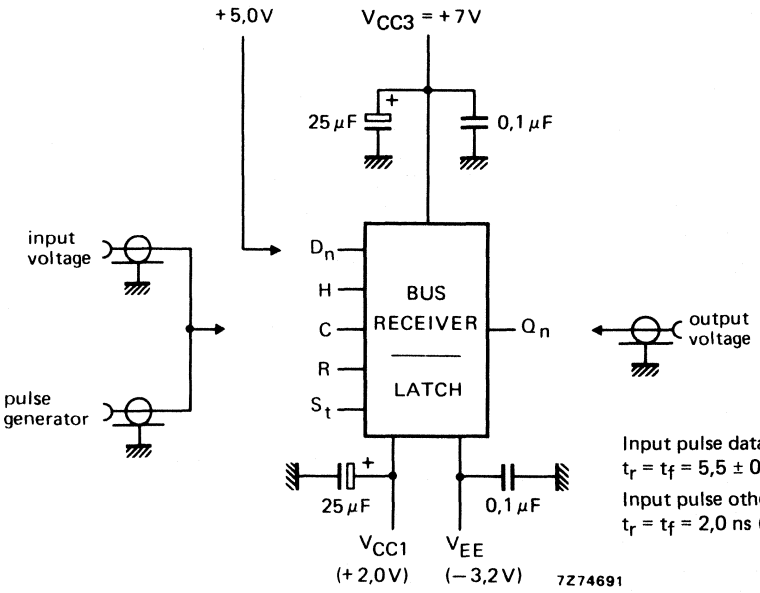
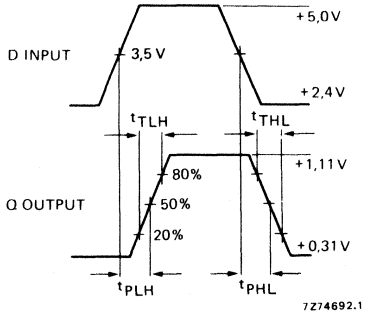


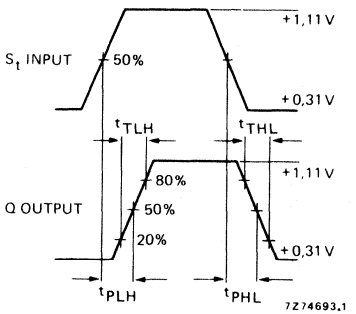
Fig. 6 Switching time test circuit

Switching times waveforms



inputs		
C	R	S_t
L	L	H

Fig. 7 Data to output waveforms.



inputs		
D	C	R
H	L	L

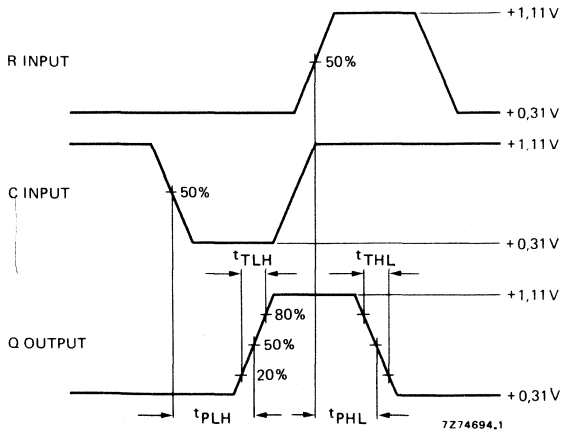
Fig. 8 Strobe to output waveforms.

D.C. CHARACTERISTICS

V_{CC1} = (ground); V_{EE} = –5.2 V; V_{CC3} = +5 V

	symbol	T_{amb} (°C)			unit	conditions
		–30	+25	+85		
Supply current negative	I_{EEmax}	167 189	152 172	167 189	mA mA	Pin 5 to ground (*) Pin 5 to V_{EE} (*)
Supply current positive	I_{CCmax}	8	8	8	mA	Pin 5 to V_{EE} V_{IL} to all data inputs
Input current data (Pins 4,6,7,13)	I_{CBOmax}	1,5	1,0	1,0	μA	Pin 5 to V_{EE} V_{IL} to data inputs one at a time. Other inputs open
Data (Pins 4,6,7,13)	I_{IHmax}	150	95	95	μA	
Reset (Pin 10)		720	450	450	μA	
Clock (Pin 11)		390	245	245	μA	Pin 5 to V_{EE}
Strobe (Pin 12)		390	245	245	μA	
Input current LOW (Pins 10,11,12)	I_{ILmin}	0,5	0,5	0,3	μA	Pin 5 to ground

(*): Pin 11 to V_{IH}; all other inputs to V_{IL}.



inputs	
D	S_t
H	H

Fig. 9 Reset to output waveforms.

TEST VOLTAGE TABLE

Operation and limits shown also apply for V_{CC} = +6.0 V

									VOLTAGE VALUES FOR TEST (Volts)																		
									10K input levels				TTL input levels (1)				hysteresis mode				V_{CC}	V_{EE}	GND		
									V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILmax}	V_{IHA}	V_{ILB}	V_{IHB}	V_{ILA}	$V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$					
							Temperature	−30°C	−0,890	−0,890	−1,205	−1,500	3,000	0,400	2,000	0,800	2,900	2,000	2,200	1,300	+5,0	−5,2	0		N
								+ 25°C	−0,810	−1,850	−1,105	−1,475	3,000	0,400	2,000	0,800	2,600	1,700	1,900	1,000	+5,0	−5,2	0		O
								+ 85°C	−0,700	−1,825	−1,035	−1,440	3,000	0,400	2,000	0,800	2,300	1,400	1,600	0,700	+5,0	−5,2	0		T
			Test limits																								E
			−30°C		+25°C		+85°C																				S
level	symbol	pin	min.	max.	min.	max.	min.	max.	unit	Applied to pins below:																	
output voltage HIGH	V_{OH}	2	−1,060	− 9,80	− 9,60	− 8,10	− 8,90	−0,700	V	pin 12	10,11			4									9	5,8	1,16		
		3	−1,060	− 9,80	− 9,60	− 8,10	− 8,90	−0,700	V	pin 12	10,11			6									9	5,8	1,16		
		2	−1,060	− 9,80	− 9,60	− 8,10	− 8,90	−0,700	V	pin 12	10,11			4									9	8	1,5,16		
		3	−1,060	− 9,80	− 9,60	− 8,10	− 8,90	−0,700	V	pin 12	10,11			6									9	8	1,5,16		
output voltage LOW	V_{OL}	2	−1,890	−1,675	−1,850	−1,650	−1,825	−1,615	V	pin 12	10,11				4								9	5,8	1,16		
		3	−1,890	−1,675	−1,850	−1,650	−1,825	−1,615	V	pin 12	10,11				6								9	5,8	1,16		
		2	−1,890	−1,675	−1,850	−1,650	−1,825	−1,615	V	pin 12	10,11				4								9	8	1,5,16		
		3	−1,890	−1,675	−1,850	−1,650	−1,825	−1,615	V	pin 12	10,11				6								9	8	1,5,16		
output threshold voltage HIGH	V_{OHC}	2	−1,060		−0,980		−0,910		V	11,12			10	4									9	5,8	1,16	(2)	
		2	−1,060		−0,980		−0,910		V		10,11	12		4									9	5,8	1,16		
		2	−1,060		−0,980		−0,910		V	10,11			11	4									9	5,8	1,16		
		2	−1,060		−0,980		−0,910		V	pin 12	10,11					4							9	5,8	1,16		
		2	−1,060		−0,980		−0,910		V	pin 12	10,11							4					9	8	1,5,16	(3)	
		2	−1,060		−0,980		−0,910		V	pin 12	10,11									4			9	8	1,5,16	(4)	
output threshold voltage LOW	V_{OLC}	2		−1,655		−1,630		−1,595	V	11,12			10	4									9	5,8	1,16	(2)	
		2		−1,655		−1,630		−1,595	V		10,11		12	4									9	5,8	1,16		
		2		−1,655		−1,630		−1,595	V	10,11			11	4									9	5,8	1,16	(2)	
		2		−1,655		−1,630		−1,595	V	pin 12	10,11					4							9	5,8	1,16		
		2		−1,655		−1,630		−1,595	V	pin 12	10,11							4					9	8	1,5,16	(3)	
		2		−1,655		−1,630		−1,595	V	pin 12	10,11									4			9	8	1,5,16	(4)	

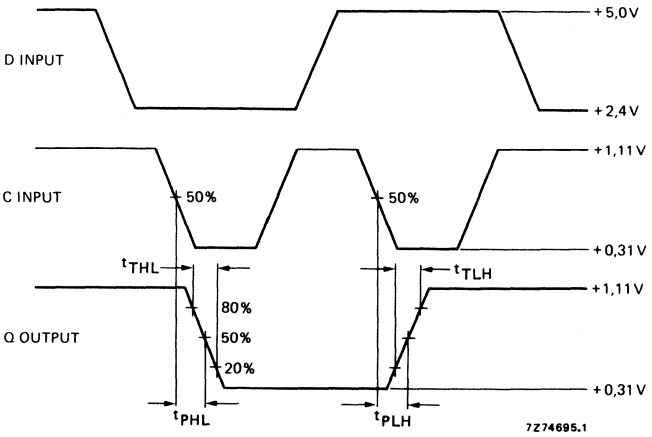
(1): For test, either IBM or TTL input levels can be chosen;
(2): Output latched for logic high state prior to test;
(3): Input level on data taken from +0,4 V up to voltage level given;
(4): Input level on data taken from +0,4 V down to voltage level given.

A.C. CHARACTERISTICS

V_{CC1} = (ground) = +2.0 V; V_{CC3} = +7.0 V; V_{EE} = −3.2 V

	symbol	pin under	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay time							
D → Q	t_{PLH}	min.	3,7	3,7	3,7	ns	input 3.5 V to 50%
	t_{PHL}	max.	15,0	15,0	40,0	ns	output (see Fig. 7)
C → Q	t_{PLH}	min.	2,7	2,7	2,7	ns	50% to 50%
	t_{PHL}	max.	11,0	9,0	11,0	ns	(see Fig. 9)
S_t → Q	t_{PLH}	min.	1,6	1,6	1,6	ns	50% to 50%
	t_{PHL}	max.	8,0	7,0	8,0	ns	(see Fig. 8)
R → Q	t_{PHL}	min.	2,0	2,0	2,0	ns	50% to 50%
		max.	8,0	6,5	8,0	ns	(see Fig. 9)
Rise time	t_{TLH}	min.	1,5	1,5	1,5	ns	between 20% and 80%
		max.	5,0	4,3	5,0	ns	
Fall time	t_{THL}	min.	1,5	1,5	1,5	ns	
	t_{THL}	max.	5,0	4,3	5,0	ns	
Set-up time							
D → C	t_s	min.	27	20	27	ns	between 50% (see Fig. 11)
Hold time							
D → C	t_h	min.	0	−2	−2	ns	
Hysteresis mode							
Rise propagation delay time							
D → Q	t_{PLH}	min.	6,6	6,7	6,6	ns	input 3.5 V to 50%
		max.	30,0	25,0	30,0	ns	output (see Fig. 7)
Fall propagation delay time							
D → Q	t_{PHL}	min.	3,7	3,7	3,7	ns	input 3.5 V to 50%
		max.	17,0	15,0	40,0	ns	output (see Fig. 7)
Set-up time	t_s	min.	30,0	25,0	30,0	ns	between 50% (see Fig. 11)
Hold time	t_h	min.	0	−2,0	−2,0	ns	

Switching times waveforms



inputs	
R	S_t
L	H

Fig. 10 Clock to output waveforms.

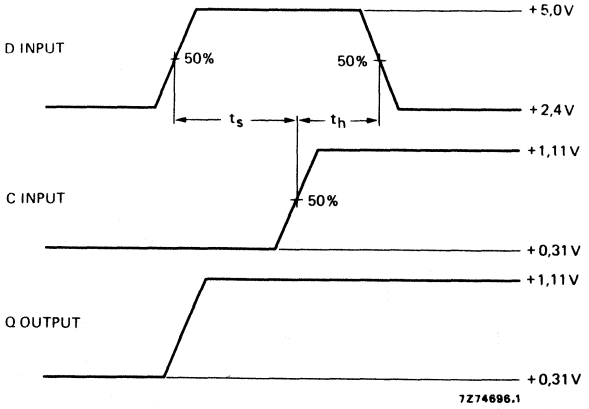


Fig. 11 Set-up and hold times waveforms.

DUAL D-TYPE LATCH

The 10130 is a clocked dual D-type latch. Each element can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is high. All unused inputs must be tied to V_{IL} or V_{EE}.

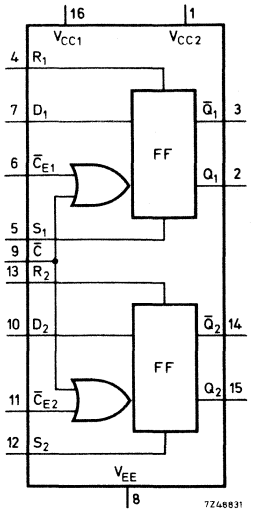


Fig. 1 Logic diagram.

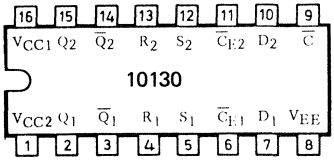


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	110 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10130N: plastic 16-lead dual in-line (SOT-38).
10130F: ceramic 16-lead dual in-line (SOT-74).

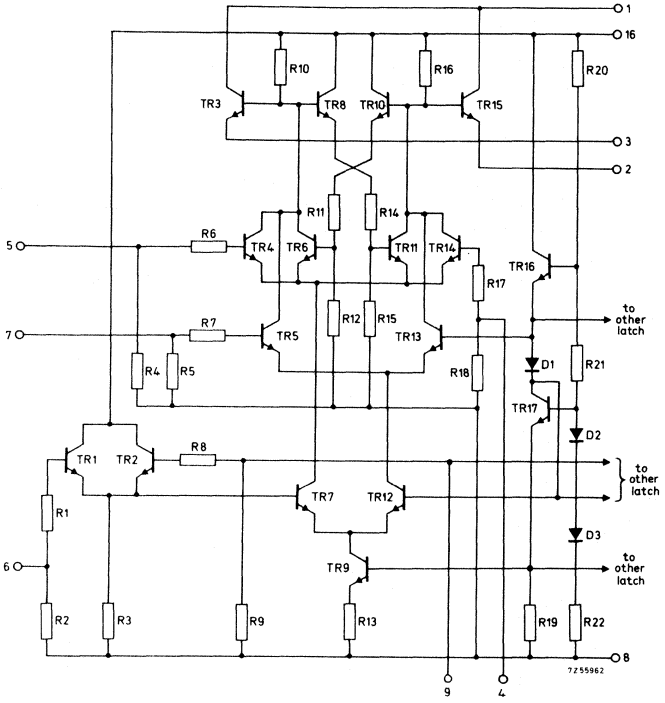
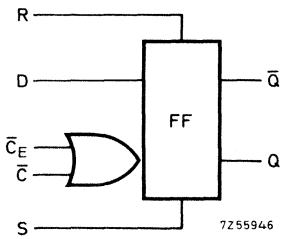


Fig. 3 Circuit diagram (one latch).



Synchronous operation

D_n	$\overline{C}$	$\overline{C_E}$	Q_{n+1} *
L	L	L	L
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	H
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

* R and S = LOW

Asynchronous operation
($\overline{C}$ or $\overline{C_E}$ = HIGH)

R	S	Q_1
L	L	Q
L	H	H
H	L	L
H	H	**

** not allowed

HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

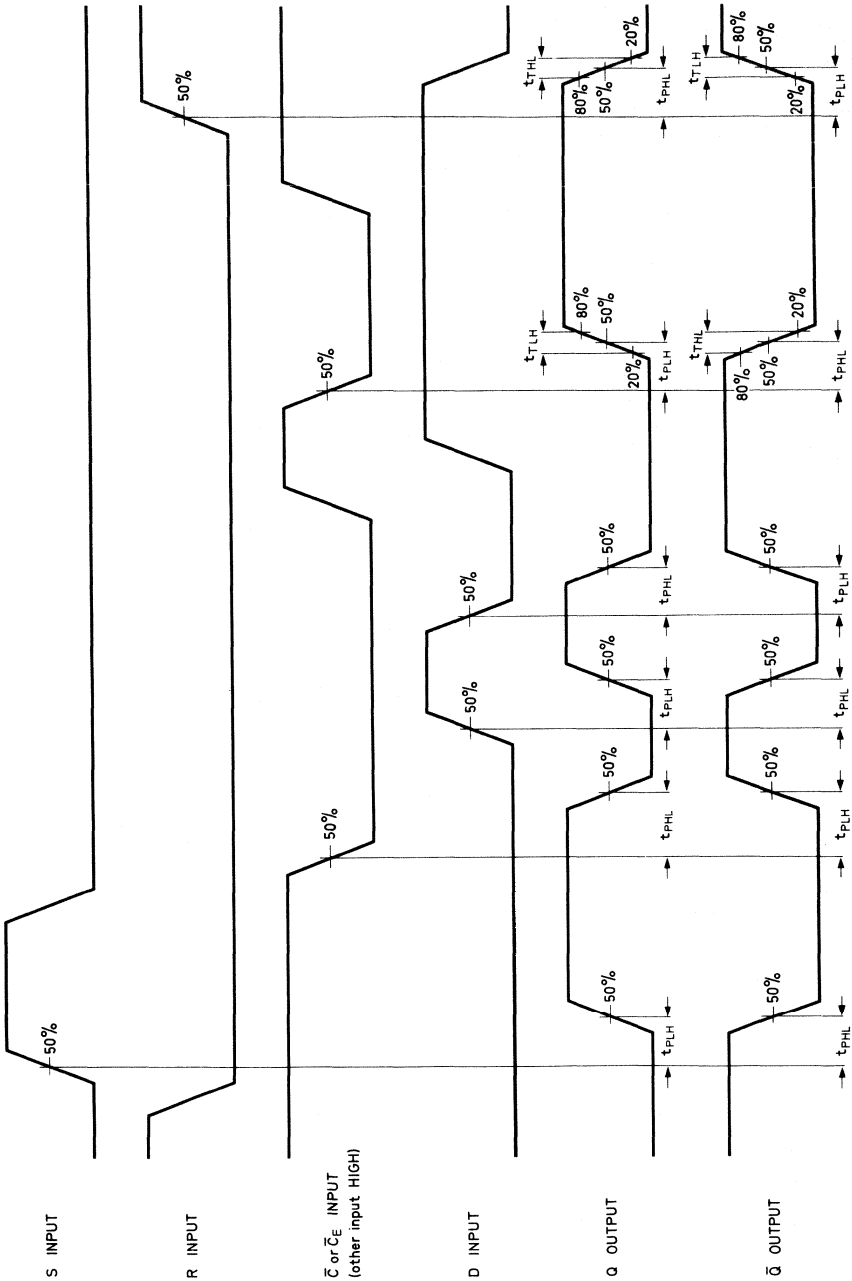


Fig. 5 Switching times waveforms. For input signals $t_{TLH} = t_{THL} = 2{,}0$ ns (between 20% and 80%); $V_{IH} = +1{,}1$ V; $V_{IL} = +0{,}3$ V.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	38	35	38	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	6,11	350	220	220	μA	
		9	425	265	265	μA	
		other inputs	455	285	285	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	S at V_{IHmax}
		typ.		− 880		mV	R at V_{ILmin}
		max.	− 890	− 810	− 700	mV	or
							D at V_{IHmax}
							$\overline{C}$, $\overline{CE}$ at V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	R at V_{IHmax}
		typ.		−1 720		mV	S at V_{ILmin}
		max.	−1 675	−1 650	−1 615	mV	or
							D at V_{ILmin}
							$\overline{C}$, $\overline{CE}$ at V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	S at V_{IHC}
							or
							D at V_{IHC}
							$\overline{C}$, $\overline{CE}$ at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	R at V_{IHC}
							or
							D at V_{ILC}
							$\overline{C}$, $\overline{CE}$ at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise and fall propagation delay times	t_{PLH}/t_{PHL}						
D → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,8	ns	
R → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,9	ns	see Waveforms Fig. 5
S → Q		min.	1,0	1,0	1,0	ns	
		max.	3,6	3,5	3,9	ns	
C → Q		min.	1,0	1,0	1,0	ns	
		max.	4,3	4,0	4,1	ns	
Rise and fall transition times	t_{TLH}/t_{THL}	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,5	3,8	ns	
Set-up time							
D → C	t_s	min.	2,5	2,5	2,5	ns	
Hold time							
D → C	t_h	min.	1,5	1,5	1,5	ns	

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP

The 10131 is a dual master-slave D-type flip-flop. Each flip-flop can be clocked separately by holding the common clock in the LOW state and using the clock enable inputs for the clocking function. The output states of the flip-flops change when the level of the clock is high. All unused inputs must be tied LOW to V_{IL} or V_{EE}.

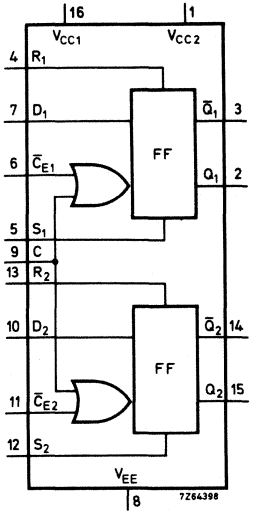


Fig. 1 Logic diagram.

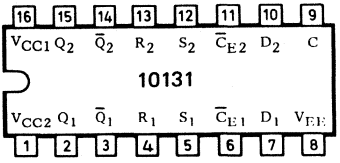


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Clock frequency	f_C	typ.	160 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	230 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10131N: plastic 16-lead dual in-line (SOT-38).
10131F: ceramic 16-lead dual in-line (SOT-74).

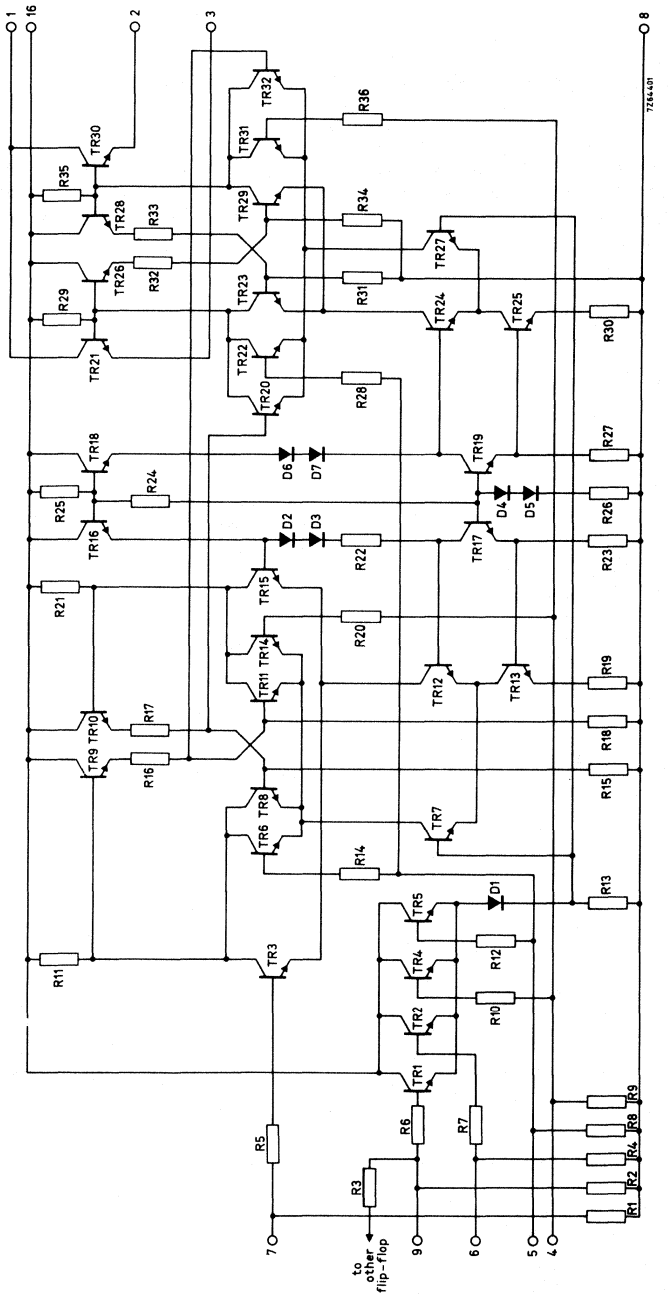
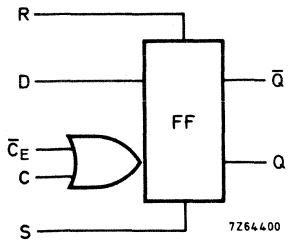


Fig. 3 Circuit diagram.



Synchronous operation

D_n	C	$\overline{C_E}$ *	Q_{n+1} **
L	L	L	Q_n
L	L	H	Q_n
L	H	L	L
L	H	H	Q_n
H	L	L	Q_n
H	L	H	Q_n
H	H	L	H
H	H	H	Q_n

Asynchronous operation

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N

Positive logic:

HIGH state = 1
LOW state = 0
N = not allowed.

Fig. 4 Logic function (one flip-flop).

* Conditions for C and $\overline{C_E}$ may be interchanged. In this table $\overline{C_E}$ is static, while for C a H represents a transition from L to H between t_n and t_{n+1}.

** R + S = LOW.

RATINGS see Family Specifications.

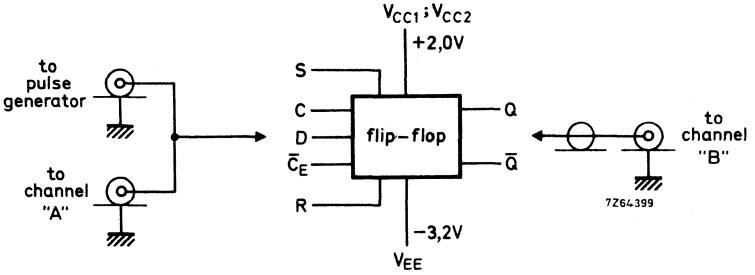


Fig. 5 Measurement of propagation delay.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	62	56	62	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section
Input current HIGH	I_{IHmax}	4,5,12,13	525	330	330	μA	
		6,11	350	220	220	μA	
		7,10	390	245	245	μA	
		9	425	265	265	μA	

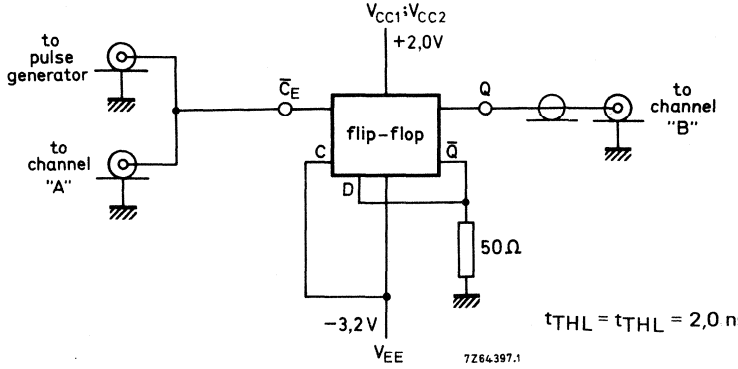
*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	S at V_{IHmax} or
		typ.		− 880		mV	R at V_{ILmin}
		max.	− 890	− 810	− 700	mV	D at V_{ILmax}
							$\overline{CE}$ at V_{ILmin}
							C at $V_{IL} \rightarrow V_{IH}$
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	S at V_{ILmin} or
		typ.		−1 720		mV	R at V_{IHmax}
		max.	−1 675	−1 650	−1 615	mV	D at V_{ILmin}
							$\overline{CE}$ at V_{ILmin}
							C at $V_{IL} \rightarrow V_{IH}$
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	S at V_{IHC} or
							R at V_{ILC}
							D at V_{IHC}
							$\overline{CE}$ at V_{ILC}
							C at $V_{ILC} \rightarrow V_{IHC}$
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	S at V_{ILC} or
							R at V_{IHC}
							D at V_{ILC}
							$\overline{CE}$ at V_{ILC}
							C at $V_{ILC} \rightarrow V_{IHC}$

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise and fall propagation delay times							
S → Q	t_{PLH}	min.	1,7	1,8	1,8	ns	
		max.	4,4	4,3	4,8	ns	
R → Q	t_{PLH}	min.	1,7	1,8	1,8	ns	see Fig. 5 and 7
		max.	4,4	4,3	4,8	ns	
C → Q	t_{PLH}	min.	1,7	1,8	1,8	ns	
		max.	4,6	4,5	5,0	ns	
Fall propagation delay time							
S → Q	t_{PHL}	min.	1,7	1,8	1,8	ns	
		max.	4,4	4,3	4,8	ns	
R → Q	t_{PHL}	min.	1,7	1,8	1,8	ns	see Fig. 5 and 7
		max.	4,4	4,3	4,8	ns	
C → Q	t_{PHL}	min.	1,7	1,8	1,8	ns	
		max.	4,6	4,5	5,0	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,1	ns	
		max.	4,6	4,5	4,9	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	4,6	4,5	4,9	ns	
Set-up time	t_s	min.	2,5	2,5	2,5	ns	see Fig. 7
Hold time	t_h	min.	1,5	1,5	1,5	ns	see Fig. 7
Clock frequency	f_c	min.	125	125	125	MHz	see Fig. 6



$t_{THL} = t_{THL} = 2{,}0$ ns (20% to 80%).

Fig. 6 Switching times test circuit. Measurement of clock frequency.

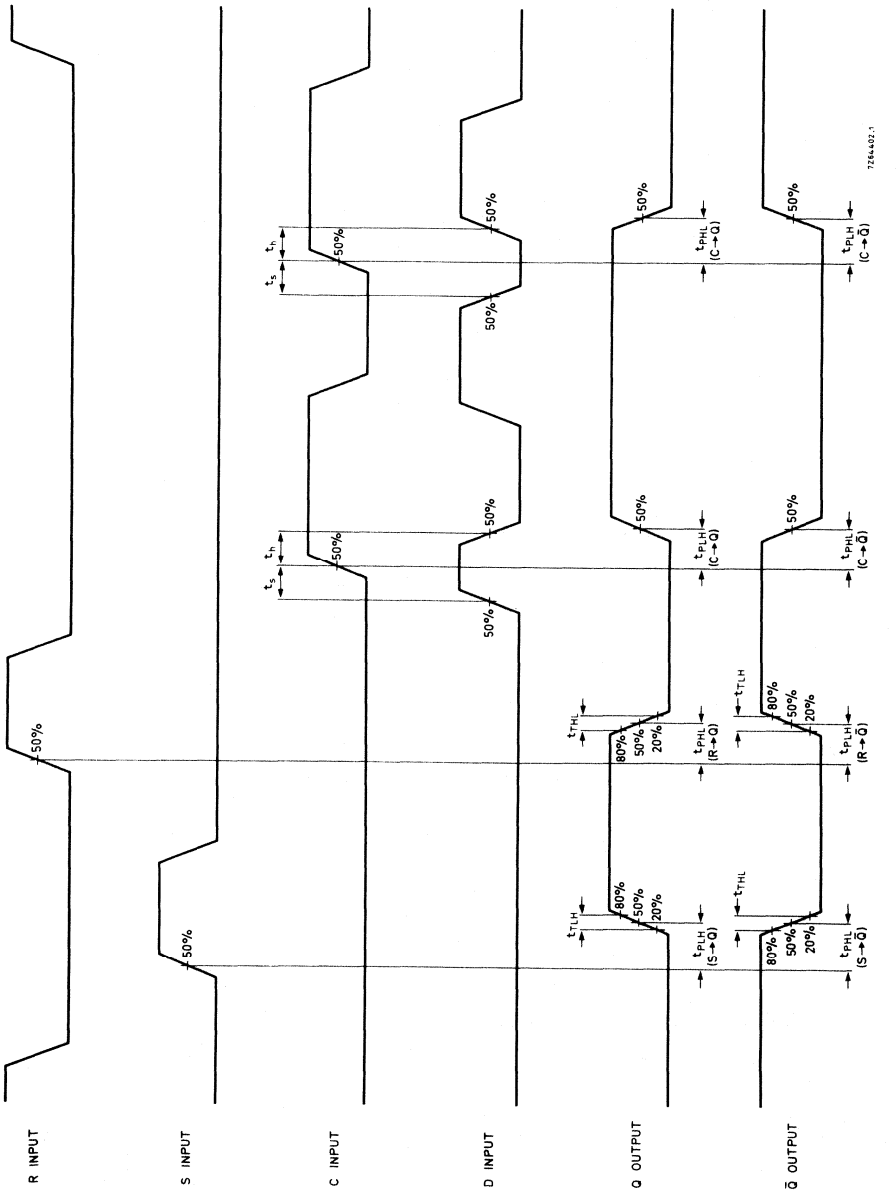


Fig. 7 Switching times waveforms. $V_{IH} = +1{,}11$ V; $V_{IL} \doteq 0{,}31$ V.

DUAL MULTIPLEXER WITH D-TYPE LATCHES

The 10132 is a dual 2-input multiplexer with clocked D-type latches and common reset. Latches can be clocked by the common clock (C) when the clock enable input (C_E) is LOW or by the clock enable input when the common clock is held in the LOW state. The outputs are latched by the positive transition of the clock (leading edge). Any change in the data input will be registered at the output only if the clock is LOW. Data inputs are selected by a common data select input (D_S).
All unused inputs must be tied LOW to V_{IL} or V_{EE}.

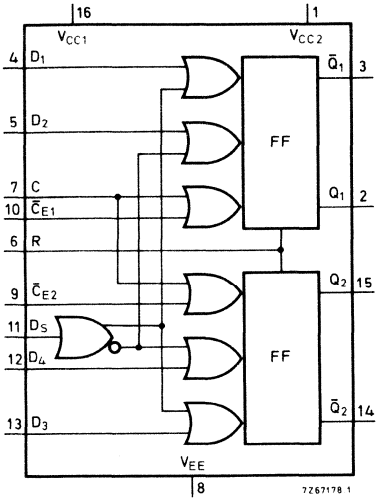


Fig. 1 Logic diagram.

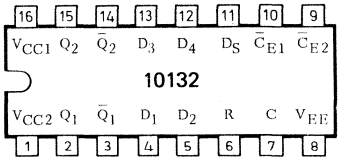


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	210 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10132N: plastic 16-lead dual in-line (SOT-38).
10132F: ceramic 16-lead dual in-line (SOT-74).

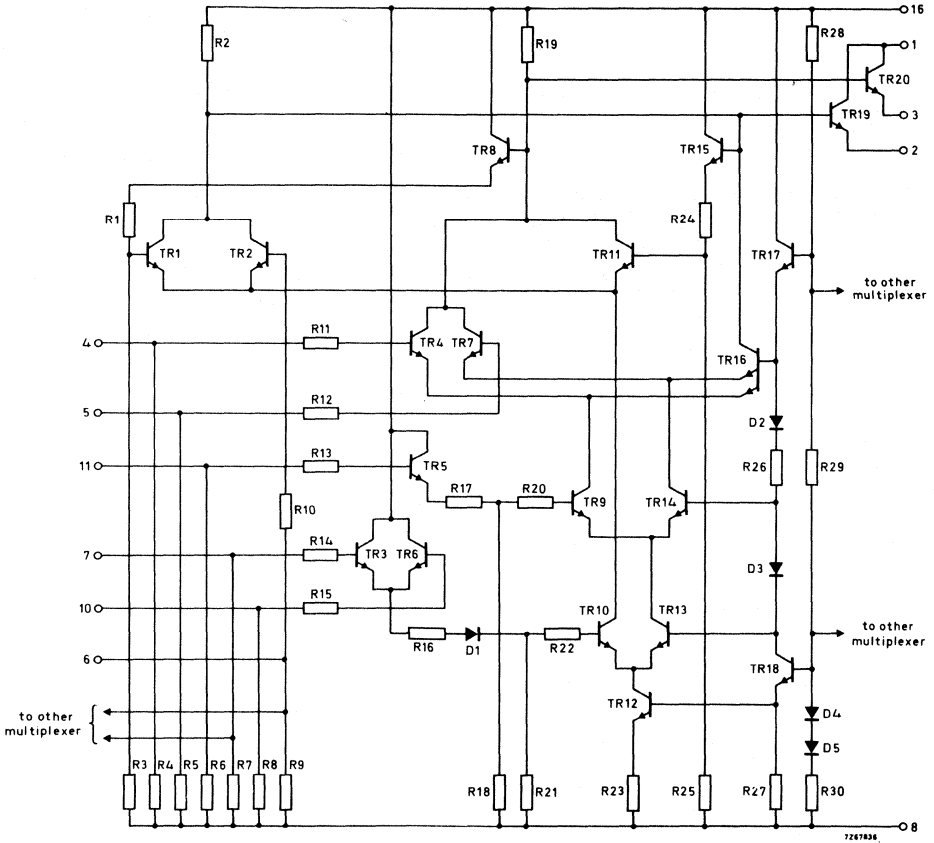


Fig. 3 Circuit diagram (one multiplexer).

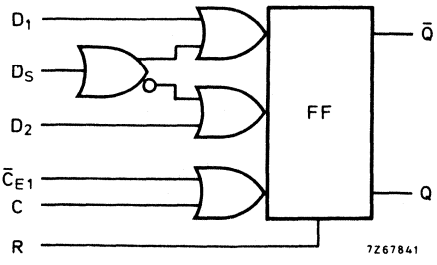


Fig. 4 Logic function.

R	D_S	C	$\bar{C}_E$	Q_{n+1}
L	L	L	L	D_1
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
L	H	L	L	D_2
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	X	X	H	L
H	X	H	X	L
H	X	L	L	Q_n

For **switching times test circuit** see Family Specifications.

Notes

1. Any change on the data input will be registered at the output only if the clock is LOW.
2. Outputs are latched on the positive transition of the clock.
3. The reset input is enbled when the clock is HIGH.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

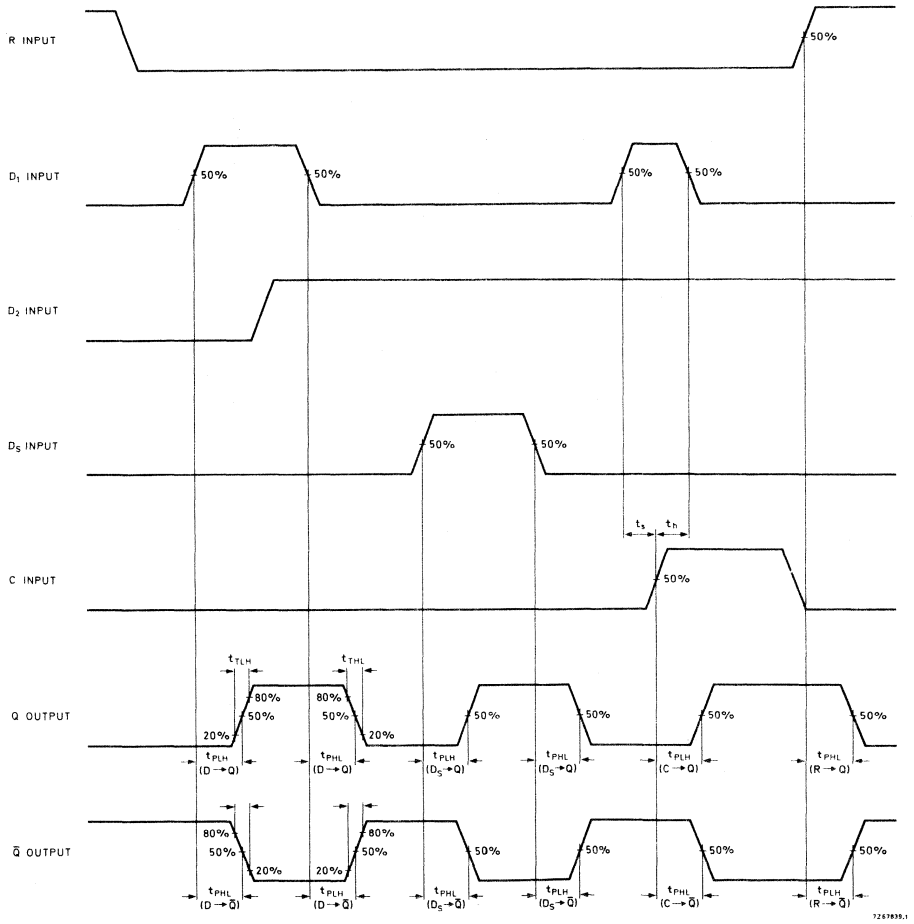


Fig. 5 Switching times waveforms. V_{IH} = + 1,11 V; V_{IL} = + 0,31 V.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	60	55	60	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	4,5,7,12,13	460	290	290	μA	
		6	620	390	390	μA	
		9,10,11	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Output 2: Pin 4 at V_{IHmax}, 9,10,11 at V_{ILmin}, 7 at V_{IL} or: 5,11 at V_{IHmax} 9,10 at V_{ILmin} 7 at V_{IL}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Output 2,15: Pins 4, 9,10,11 at V_{ILmin}, Pin 7 at V_{IL} or: 5,9,10 at V_{ILmin} 11 at V_{IHmax} 7 at V_{IL}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	Output 2: Pin 4 at V_{IHC}, 7,9,10,11 at V_{ILC} or: 5,11 at V_{IHC} 7,9,10 at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	Output 2,15: Pins 4, 7,9,10,11 at V_{ILC} or: 11 at V_{IHC} 5,7,9,10 at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay time							
D → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
	t_{PHL}	max.	3,6	3,3	3,7	ns	
R → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
	t_{PHL}	max.	4,0	3,8	4,2	ns	for Waveforms see Fig. 5
C → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	
	t_{PHL}	max.	6,0	5,7	6,3	ns	
D_s → Q	t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	4,8	4,6	5,0	ns	
Rise time	t_{TLH}	min.	1,5	1,5	1,5	ns	
		max.	3,7	3,5	3,8	ns	between 20% and 80%
Fall time	t_{THL}	min.	1,5	1,5	1,5	ns	
		max.	3,7	3,5	3,8	ns	
Set-up time							
D → C	T_s	min.	2,5	2,5	2,5	ns	
D_s → C	T_s	min.	3,5	3,5	3,5	ns	
Hold time							
D → C	T_h	min.	1,5	1,5	1,5	ns	
D_s → C	T_h	min.	1,0	1,0	1,0	ns	

For switching times test circuit see Family Specifications.

Notes: 1) Any change on the data input will be registered at the output only if the clock is low.
2) Outputs are latched on the positive transition of the clock.
3) The reset input is enbled when the clock is HIGH.

QUADRUPLE LATCH

The 10133 is a quadruple latch with D-type inputs and enable outputs. Data (D) inputs are registered at the output while the clock is HIGH. Data inputs are latched by the negative transition of the clock (trailing edge).
All unused inputs must be tied LOW to V_{IL} or V_{EE}.

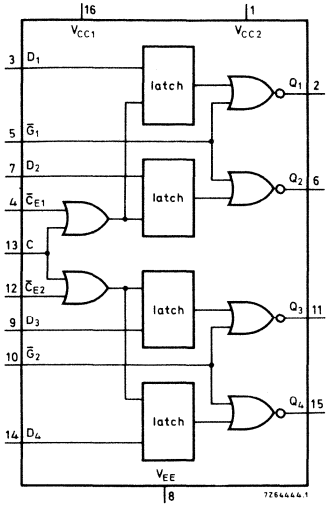


Fig. 1 Logic diagram.

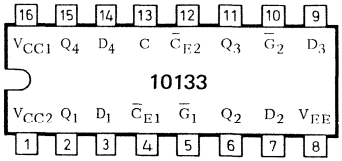


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	4.0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	310 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10133N: plastic 16-lead dual in-line (SOT-38).
10133F: ceramic 16-lead dual in-line (SOT-74).

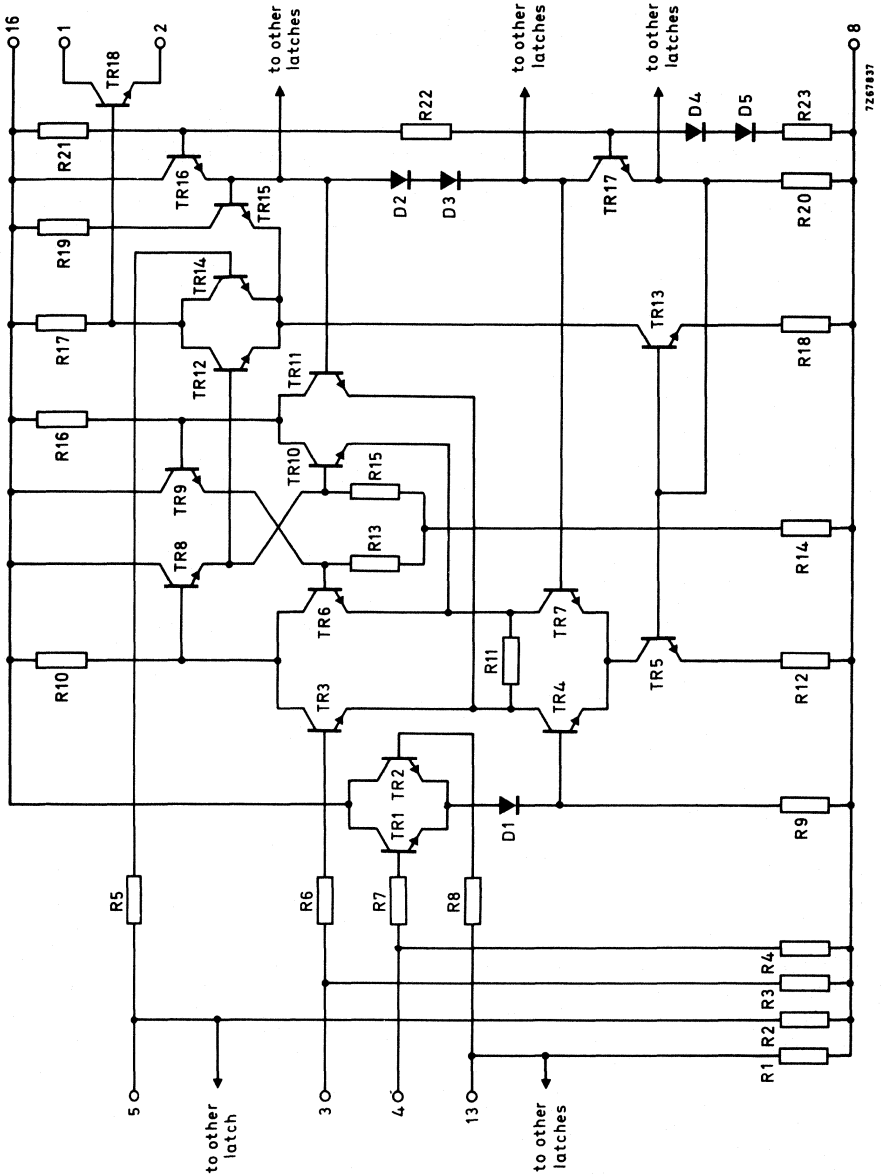


Fig. 3 Circuit diagram (one latch).

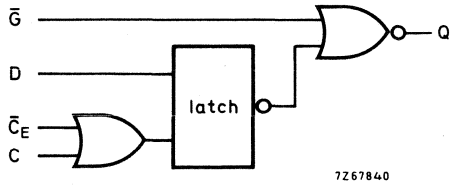


Fig. 4 Logic function.

$\overline{G}$	C	$\overline{C_E}$	D	Q_{n+1}
H	X	X	X	L
L	L	L	X	Q_n
L	L	H	L	L
L	H	L	L	L
L	H	H	L	L
L	L	H	H	H
L	H	L	H	H
L	H	H	H	H

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

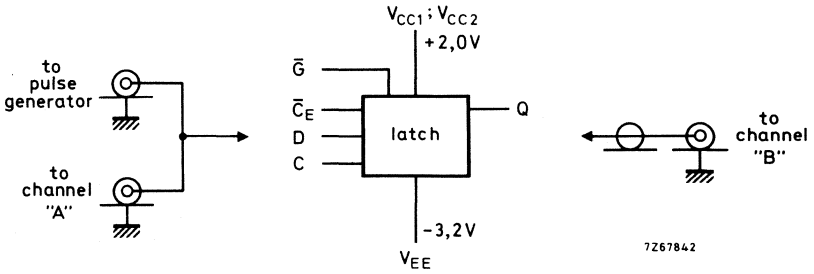


Fig. 5 Switching times test circuit.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	82	72	82	mA	
Input current LOW	I_{ILmin}	3 *	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	3,7,9,14	390	245	245	μA	
		4,12	425	265	265	μA	
		5,10,13	560	350	350	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Outputs 2,6,11,15:
		typ.		− 880		mV	Pins 3,7,9,14 at V_{IHmax}
		max.	− 890	− 810	− 700	mV	Pins 5,10 at V_{ILmin} 13 or 4,12 at V_{IHmax}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Outputs 2,6,11,15:
		typ.		−1 720		mV	Pins 5,10 at V_{IHmax}
		max.	−1 675	−1 650	−1 615	mV	or pins 3,7,9,14 at V_{ILmin} Pins 5,10 at V_{ILmin} 13 or 4,12 at V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	Outputs 2,6,11,15: 3,7,9,14 at V_{IHC} 5,10 at V_{ILC} 13 or 4,12 at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	Outputs 2,6,11,15: 5,10 at V_{IHC} or 3,7,9,14 at V_{ILC} 5,10 at V_{ILC} 13 or 4,12 at V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise propagation delay time							
D → Q	t_{TLP}	min.	1,0	1,0	1,1	ns	DATA
		max.	5,6	5,4	5,9	ns	
C → Q	t_{PLH}	min.	1,0	1,0	1,2	ns	CLOCK
		max.	5,4	5,4	6,0	ns	
G → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	GATE ENABLE
		max.	3,2	3,1	3,4	ns	
Rise time	t_{TLH}	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,5	3,8	ns	
Fall time	t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	3,6	3,5	3,8	ns	
Set-up time	T_s	min.	2,5	2,5	2,5	ns	
Hold time	T_h	min.	1,5	1,5	1,5	ns	

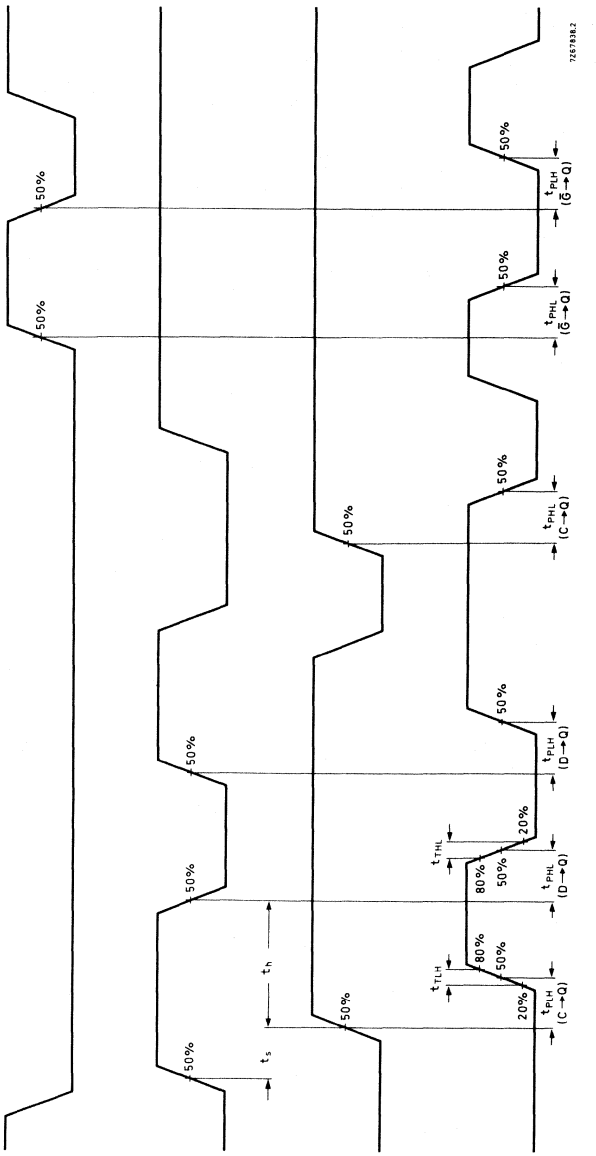


Fig. 6 Switching times waveforms. Conditions for input signals; $t_r = t_f = 2{,}0$ ns (20% to 80%); $V_{IH} = +1{,}1$ V; $V_{IL} = +0{,}3$ V.

DUAL MULTIPLEXER WITH D-TYPE LATCHES

The 10134 is a dual 2-input multiplexer with clocked D-type latches. Latches can be clocked by the common clock (C) when the clock enable input (C_E) is LOW or by the clock enable input when the common clock is held in the LOW state. The outputs are latched by the positive transition of the clock (leading edge). Any change in the data input will be registered at the output only if the clock is LOW. Data inputs are selected by two data select inputs (D_{S1} and D_{S2}).

All unused inputs must be tied LOW to V_{IL} or V_{EE}.

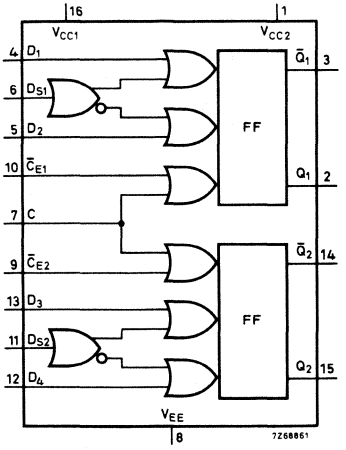


Fig. 1 Logic diagram.

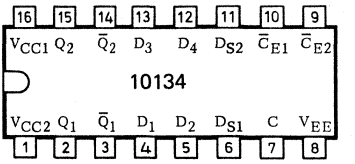


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	220 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10134N: plastic 16-lead dual in-line (SOT-38).
10134F: ceramic 16-lead dual in-line (SOT-74).

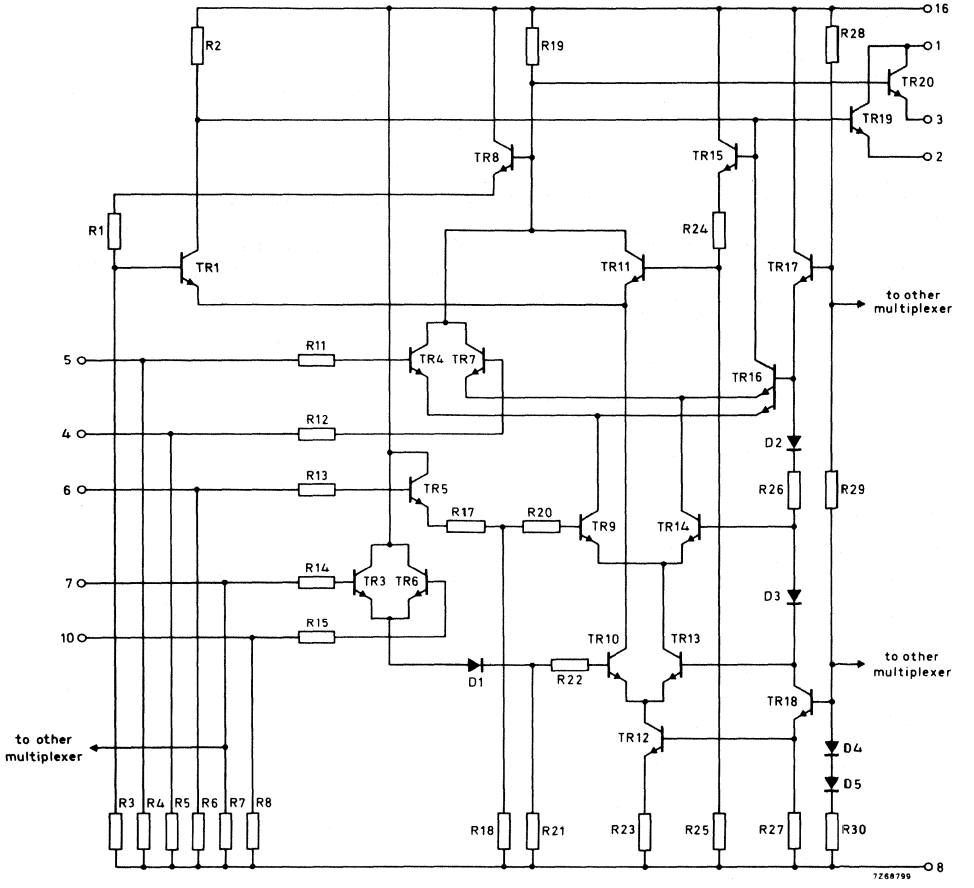


Fig. 3 Circuit diagram (one multiplexer).

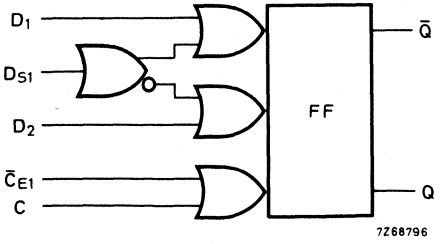


Fig. 4 Logic function.

D_S	C	$\overline{C_E}$	Q_{n+1}
L	L	L	D_1
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	D_2
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

Function table.

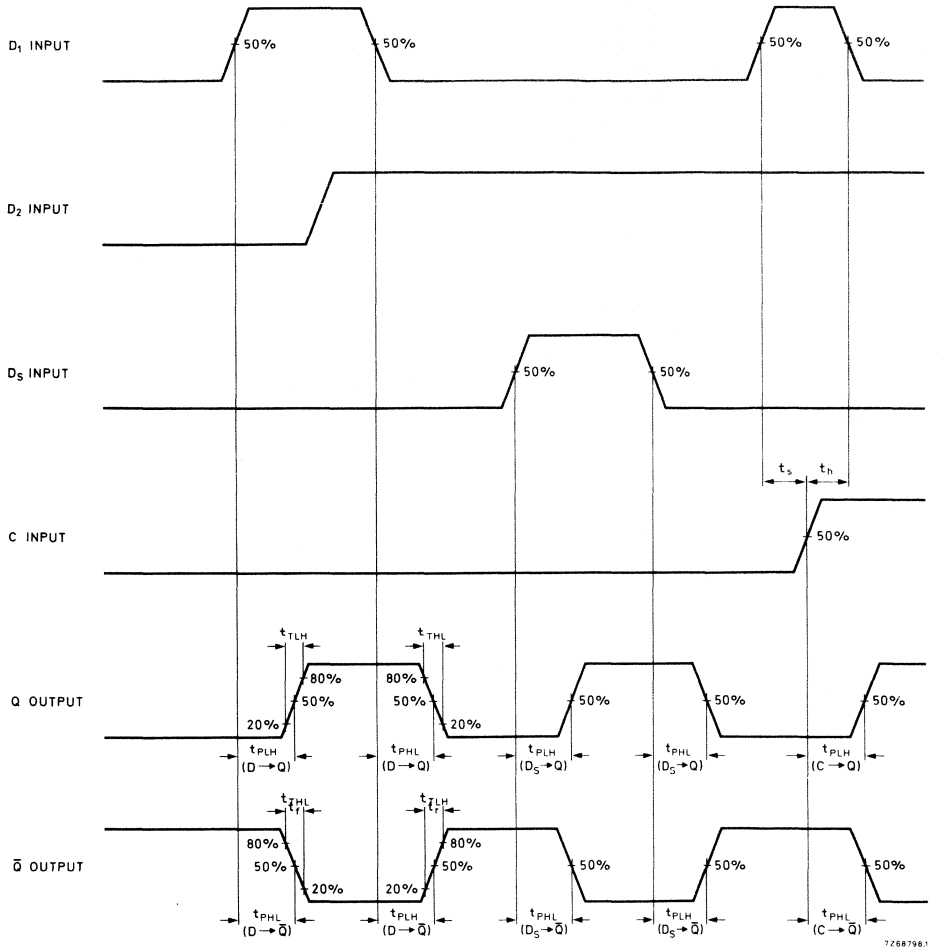


Fig. 5 Switching times waveforms.

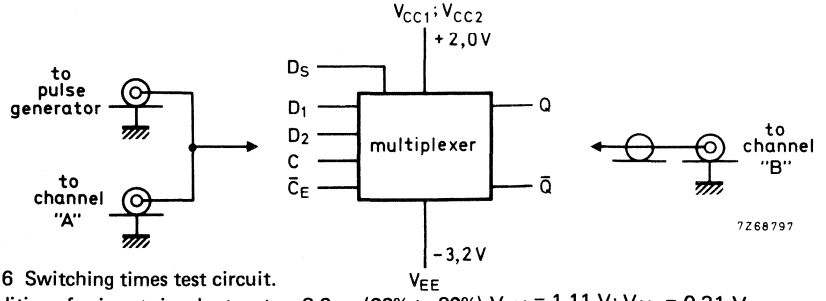


Fig. 6 Switching times test circuit.

Conditions for input signals: $t_r = t_f = 2{,}0$ ns (20% to 80%). $V_{IH} = 1{,}11$ V; $V_{IL} = 0{,}31$ V.

1. Any change on the data input will be registered at the output only if the clock is LOW
2. Outputs are latched on the positive transition of the clock.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	60	55	60	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,5	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	4,5,7,12,13 6,9,10,11	460 425	290 265	290 265	μA μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min. typ. max.	−1 060 − 890	− 960 − 880 − 810	− 890 − 700	mV mV mV	Output 2: 4 at V_{IHmax} 6,10 at V_{ILmax} 7 at V_{IL} or 5,6 at V_{IHmax} 10 at V_{ILmin} 7 at V_{IL}
Output voltage LOW	V_{OL}	min. typ. max.	−1 890 −1 675	−1 850 −1 720 −1 650	−1 825 −1 615	mV mV mV	Output 2: 4,6,10 at V_{ILmin}, 7 at V_{IL} or 5,10 at V_{ILmin} 6 at V_{IHmax} 7 at V_{IL}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	Output 2: 4 at V_{IHC} 6,7,10 at V_{ILC} or 5,6, at V_{IHC} 7,10 at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	Output 2: 4,6,7,10 at V_{ILC} or 6 at V_{IHC} 5,7,10 at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise propagation delay time							
D → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	DATA
	t_{PHL}	max.	3,5	3,3	3,6	ns	
C → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	CLOCK
	t_{PHL}	max.	6,0	5,7	6,3	ns	
D_s → Q	t_{PLH}	min.	1,0	1,0	1,0	ns	DATA SELECT
	t_{PHL}	max.	4,8	4,6	5,0	ns	
Rise/Fall time	t_{TLH}	min.	1,5	1,5	1,5	ns	between 20% and 80%
	t_{THL}	max.	3,7	3,5	3,8	ns	
Set-up time							
D → C	T_s	min.	2,5	2,5	2,5	ns	
D_s → C	T_s	min.	3,5	3,5	3,5	ns	
Hold time							
C → D	T_h	min	1,5	1,5	1,5	ns	
C → D_s	T_h	min.	1,0	1,0	1,0	ns	

DUAL JK MASTER-SLAVE FLIP-FLOP

The 10135 is a dual master-slave d.c. coupled JK flip-flop. It contains a common clock and separate $\overline{J}\,\overline{K}$ inputs which do not effect the output when the clock is static. The outputs of the GXB10135 change state with the positive transition of the clock. Asynchronous set (S) and reset (R) inputs are provided which override the clock. Unused inputs must be tied LOW to V_{IL} or V_{EE}.

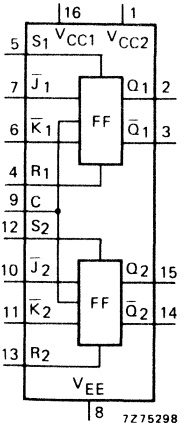


Fig. 1 Logic diagram.

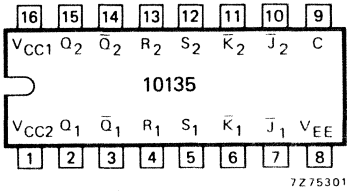


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Clock frequency	f_C	typ.	140 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	280 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10135N: plastic 16-lead dual in-line (SOT-38).
10135F: ceramic 16-lead dual in-line (SOT-74).

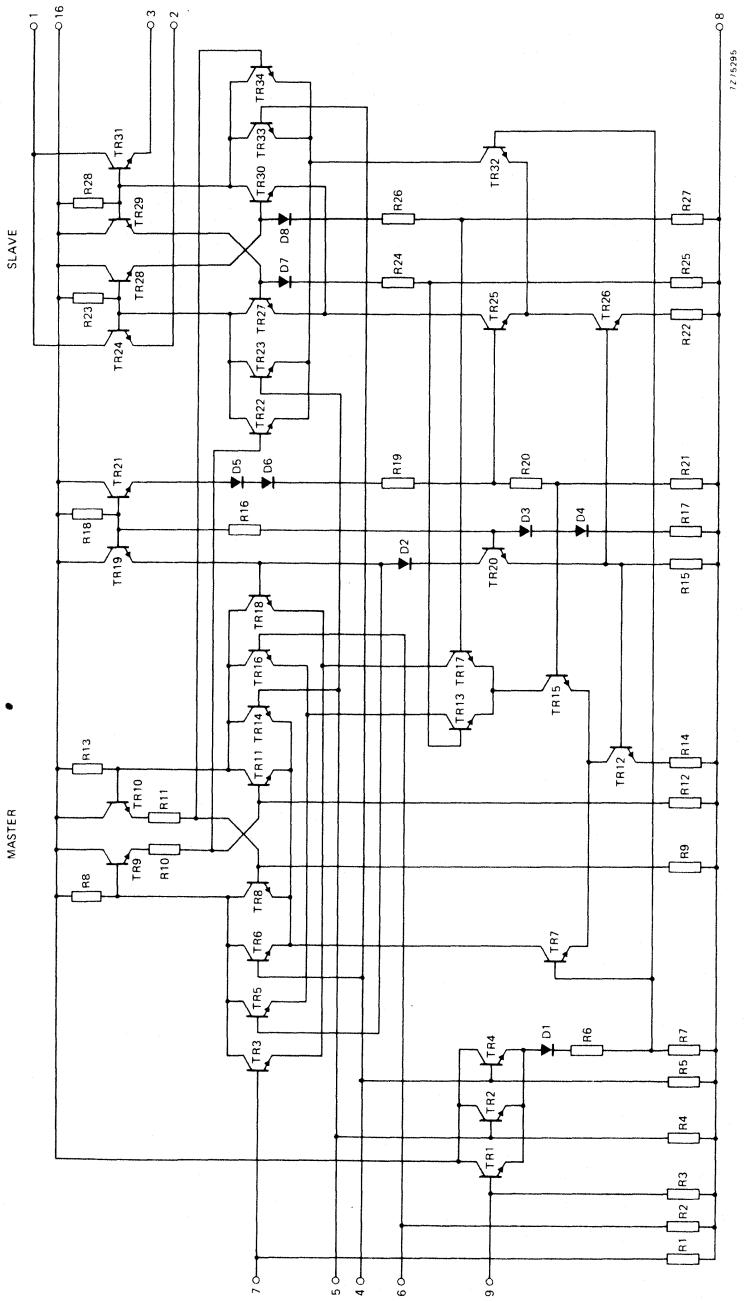


Fig. 3 Circuit diagram (one flip-flop).

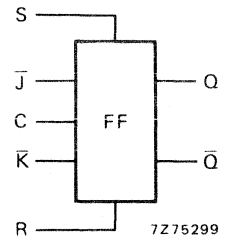


Fig. 4 Logic function.

FUNCTION TABLES

R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	*

$\overline{J}$	$\overline{K}$	R	S	$Q_n + 1$
L	L	L	L	$\overline{Q}_n$
H	L	L	L	L
L	H	L	L	H
H	H	L	L	Q_n

* Not allowed.

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications

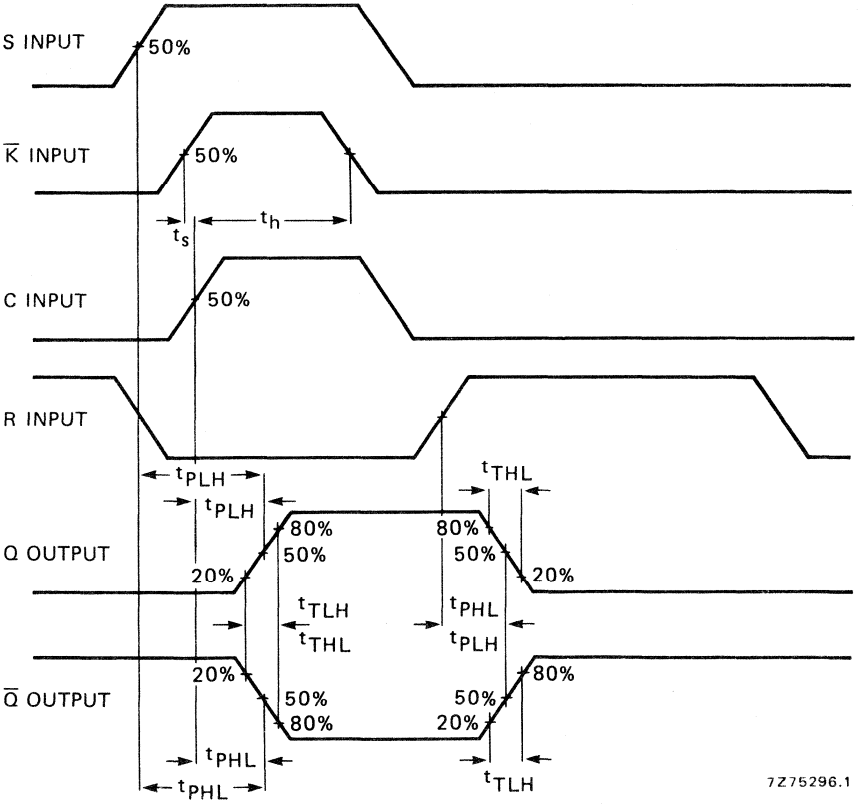


Fig. 5 Switching times waveforms; V_{IH} = 1,11 V; V_{IL} = 0,31 V.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	75	68	75	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	6,7,9,10,11	425	265	265	μA	
		4,5,12,13	620	390	390	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	All input/output combinations in accordance with the function table. Input conditions: V_{ILmin}, V_{IHmax} for V_{OH} and V_{OL} or V_{IHC}, V_{ILC} for V_{OHC} and V_{OLC}.
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Propagation delay time	t_{PLH}/t_{PHL}						
C → Q/$\overline{Q}$		min.	1,8	1,8	1,8	ns	CLOCK
		max.	5,0	4,5	4,6	ns	
S → Q/$\overline{Q}$		min	1,8	1,8	1,8	ns	SET
		max.	5,0	5,0	5,2	ns	
R → Q/$\overline{Q}$		min.	1,8	1,8	1,8	ns	RESET
		max.	5,6	5,0	5,2	ns	
Transition rise and fall times	t_{THL}/t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		max.	4,8	4,5	4,7	ns	
Set-up time	T_s	min.	2,5	2,5	2,5	ns	C $\overline{K}$
Hold time	T_h	min.	1,5	1,5	1,5	ns	
Clock frequency	F_c	min.	125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

UNIVERSAL HEXADECIMAL COUNTER

The 10136 is a high speed hexadecimal synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz.
The operation mode of the counter is programmed by three control lines (S_1, S_2 and $\overline{C}_{IN}$) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2 and D_3) to be entered into the counter.
$\overline{C}_{OUT}$ goes LOW on the terminal count, or when the counter is being preset.
The counter changes state only on the positive-going edge of the clock, so at any other time, any other input may change without any result (except for $\overline{C}_{OUT}$).
This binary counter can be used in many applications, such as in computing for high speed control processors and peripheral controllers. Unused inputs must be tied LOW to V_{IL} or V_{EE}.

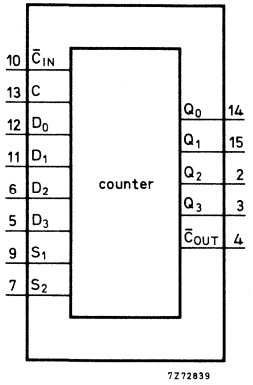


Fig. 1 Block diagram.

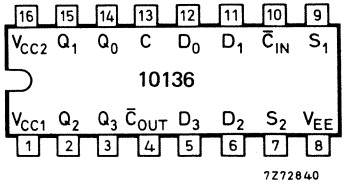


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}		−30 to + 85 °C
Clock frequency	f_C	typ.	150 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	625 mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10136N: plastic 16-lead dual in-line (SOT-38).
10136F: ceramic 16-lead dual in-line (SOT-74).

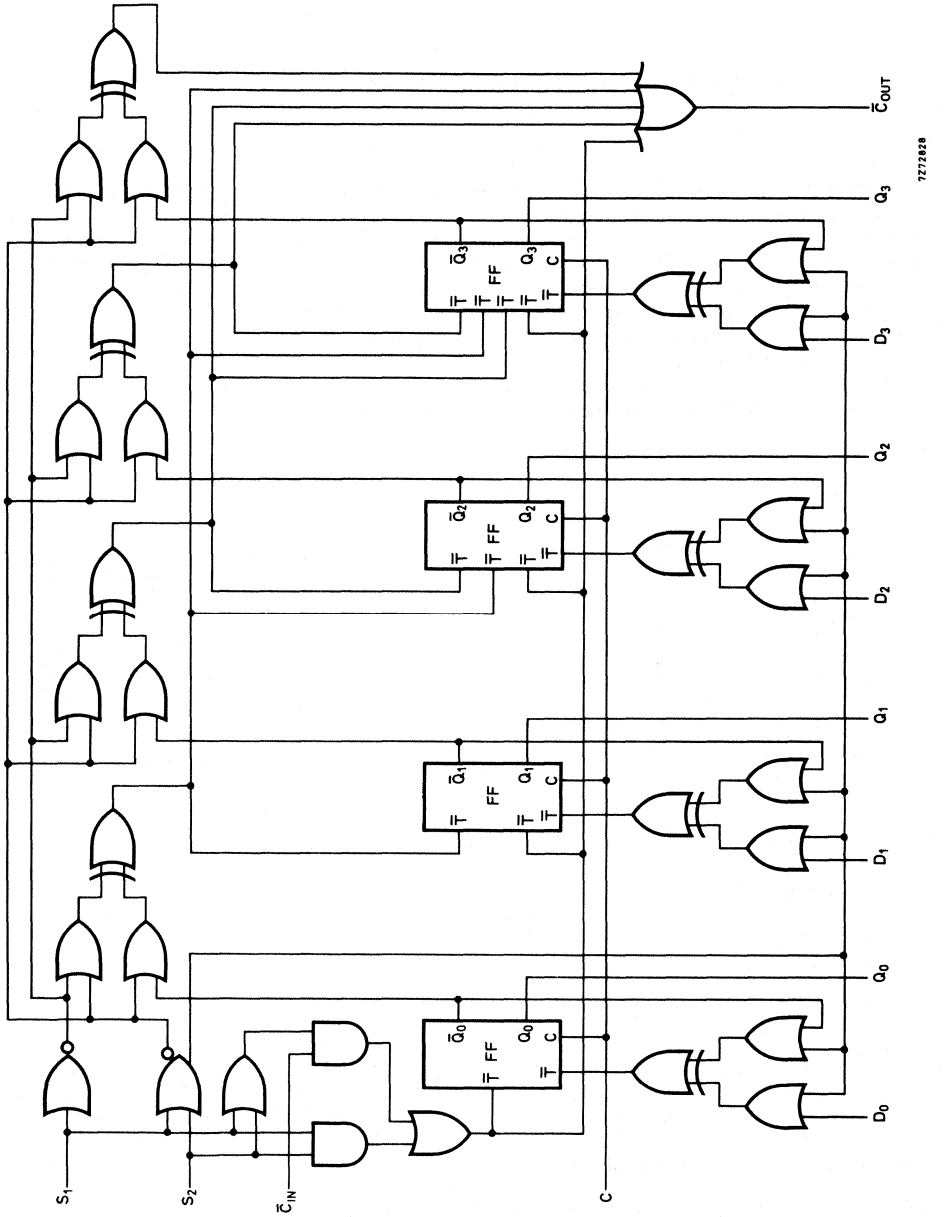


Fig. 3 Logic diagram.

FUNCTION SELECT TABLE

S_1	S_2	operating mode
L	L	preset (programme)
L	H	increment (count up)
H	L	decrement (count down)
H	H	hold (stop count)

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

SEQUENTIAL FUNCTION TABLE

inputs								outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	L	H	H	L	H	H	H
L	H	X	X	X	X	L	H	L	H	H	H	H
L	H	X	X	X	X	L	H	H	H	H	H	L
L	H	X	X	X	X	H	L	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H
H	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	H	H	H	H	H

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	165	150	165	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	5,6,11,12	350	220	220	μA	
		9,10	390	245	245	μA	
		7	425	265	265	μA	
		13	460	290	290	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For output 14, pin 12 at V_{IH} pins 7,9 at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For output 14, pins 7,9 at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For output 14, pin 12 at V_{IHC} pins 7,9 at V_{ILmin} (1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For output 14, pin 12 at V_{ILC} pins 7,9 at V_{ILmin} (1)

(1) Measure output after clock pulse appears at clock input (pin 13).

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remark
			−30	+25	+85		
Rise and fall propagation delay time							
C → Q	$\frac{t_{PLH}}{t_{PHL}}$	min.	0,8	1,0	1,4	ns	
		max.	4,8	4,5	5,0	ns	
C → $\overline{C}$OUT	$\frac{t_{PLH}}{t_{PHL}}$	min.	2,0	2,5	2,4	ns	
		max	10,9	10,5	11,5	ns	
$\overline{C}$IN → $\overline{C}$OUT	$\frac{t_{PLH}}{t_{PHL}}$	min.	1,6	1,6	1,9	ns	
		max.	7,4	6,9	7,5	ns	
Rise and fall transition time	$\frac{t_{TLH}}{t_{THL}}$	min.	0,9	1,0	1,0	ns	between 20% and 80%
		max.	3,3	3,3	3,5	ns	
Set-up time							
Dn → C	T_s	min.	3,5	3,5	3,5	ns	Fig. 4
S → C	T_s	min.	7,5	7,5	7,5	ns	
$\overline{C}$IN → C	T_s	min.	4,5	3,7	4,5	ns	Fig. 7a
C → $\overline{C}$IN	T_s	min.	−1,0	−1,0	−1,0	ns	Fig. 7c
Hold time							
C → D_n	T_h	min.	0	0	0	ns	Fig. 4
C → S	T_h	min.	−2,5	−2,5	−2,5	ns	
C → $\overline{C}$IN	T_h	min.	−1,6	−1,6	−1,6	ns	Fig. 7b
$\overline{C}$IN → C	T_h	min.	4,0	3,1	4,0	ns	Fig. 7d
Counting frequency							
Count-up	$F_c$up	min.	125	125	125	MHz	
Count-down	$F_c$down	min.	125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

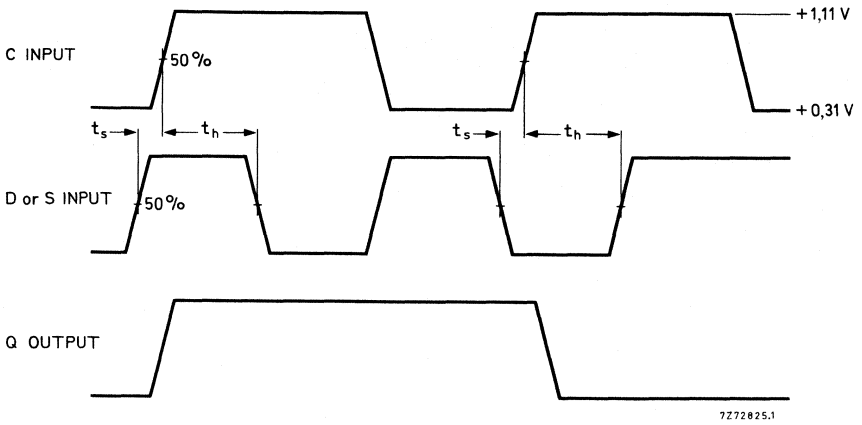


Fig. 4 Switching times waveforms.

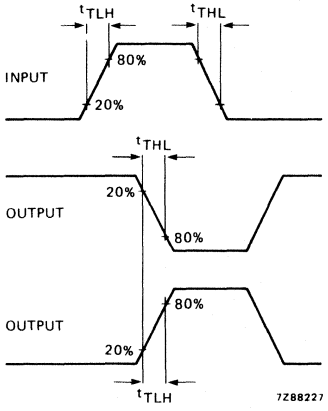


Fig. 5 Transition times (rise and fall times).

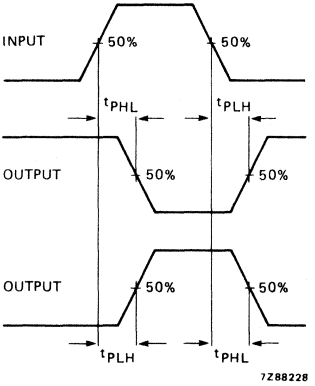


Fig. 6 Propagation delay times.

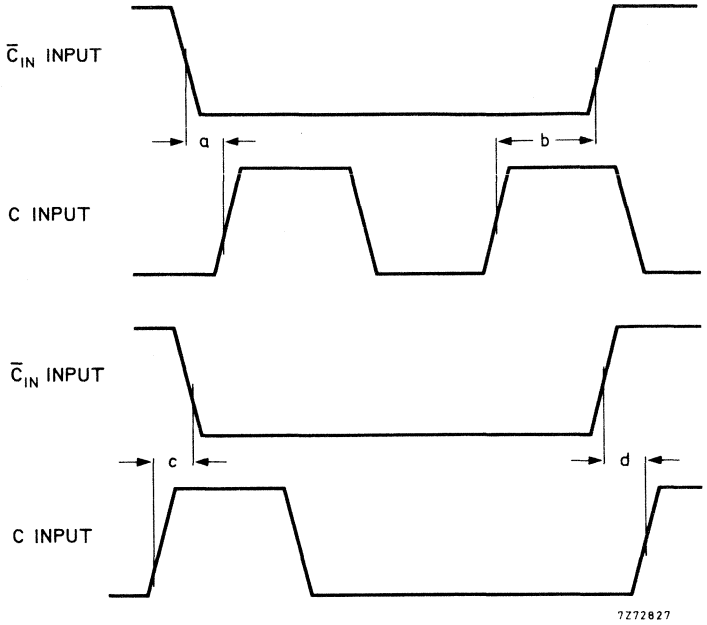


Fig. 7 Switching times waveforms (Set-up and hold).

(a) is the minimum time to wait to clock the counter after it has been enabled.

(b) is the minimum time that the counter may be clocked before it has been disabled.

(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.

(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.

(b) and (c) may be negative numbers.

UNIVERSAL DECADE COUNTER

The 10137 is a high speed synchronous decade counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The operation mode of the counter is programmed by three control lines (S_1, S_2 and $\overline{C}_{IN}$) as can be seen in the function select table. In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs (D_0, D_1, D_2 and D_3) to be entered into the counter. $\overline{C}_{OUT}$ goes LOW on the terminal count. $\overline{C}_{OUT}$ is partially decoded from Q_1 and Q_2 directly, so in the preset mode the condition of $\overline{C}_{OUT}$ after the clock's positive excursion will depend on the condition of Q_1 and/or Q_2. The counter changes state only on the positive-going edge of the clock, so at any other time, any other input may change without any result (except for $\overline{C}_{OUT}$). The sequence for counting out of improper states is as shown in the state diagrams. This binary counter can be used in many applications, such as in computing for high speed control processors and peripheral controllers. Unused inputs must be tied LOW to V_{IL} or V_{EE}.

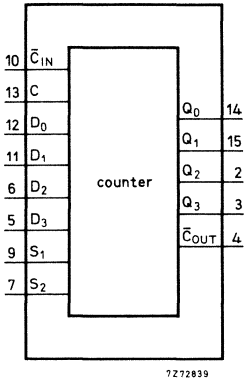


Fig. 1 Block diagram.

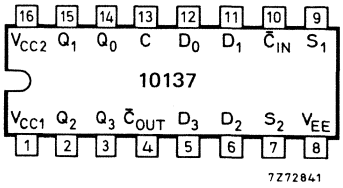


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}		−30 to + 85 °C
Counting frequency	f_C	typ.	150 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	625 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10137N: plastic 16-lead dual in-line (SOT-38).
10137F: ceramic 16-lead dual in-line (SOT-74).

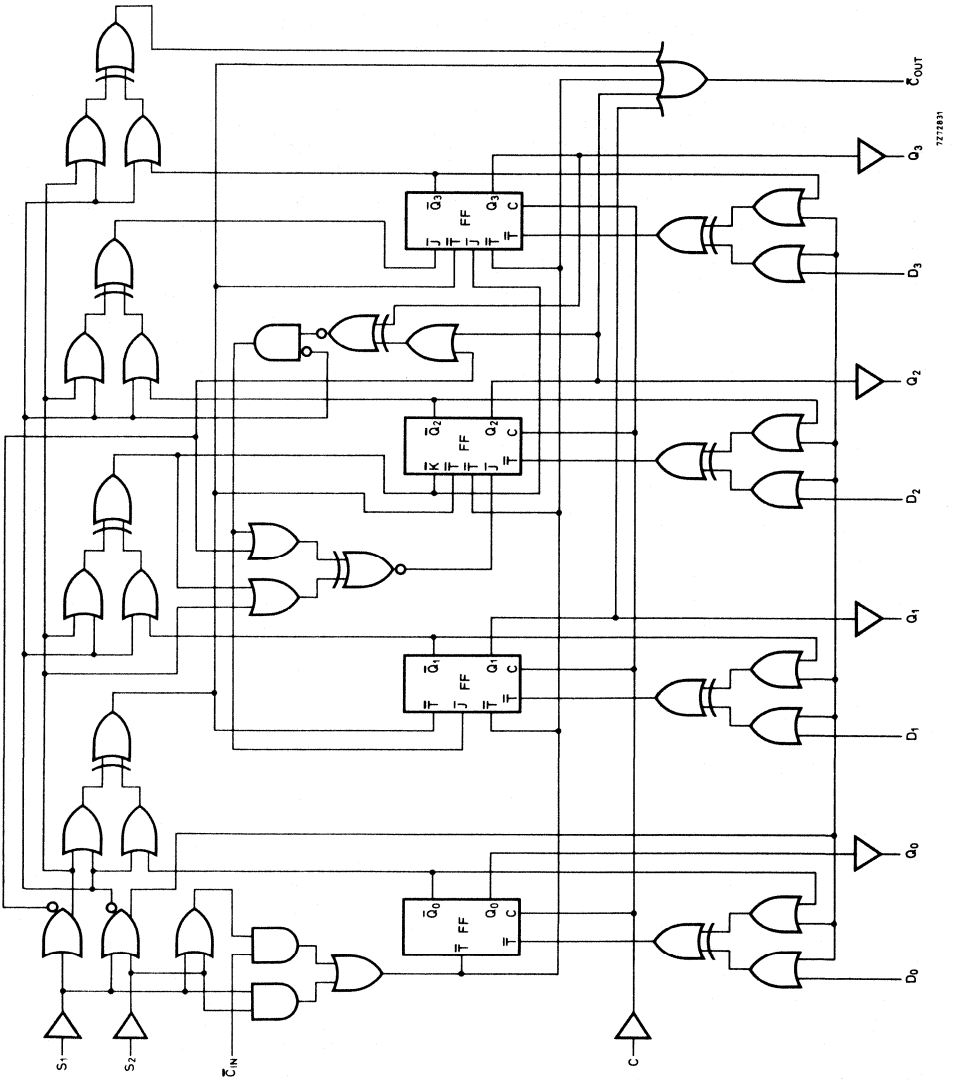


Fig. 3 Logic diagram.

Function select table

S_1	S_2	operating mode
L	L	preset (programme)
L	H	increment (count up)
H	L	decrement (count down)
H	H	hold (stop count)

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

Sequential function table

inputs								outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{C}_{IN}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{C}_{OUT}$
L	L	H	H	H	L	X	H	H	H	H	L	H
L	H	X	X	X	X	L	H	L	L	L	H	H
L	H	X	X	X	X	L	H	H	L	L	H	L
L	H	X	X	X	X	L	H	L	L	L	L	H
L	H	X	X	X	X	L	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
H	H	X	X	X	X	X	H	H	L	L	L	H
L	L	H	H	L	L	X	H	H	H	L	L	H
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L

RATINGS see Family Specifications.

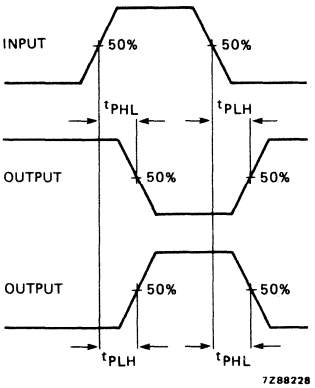


Fig. 4 Propagation delay times waveform.

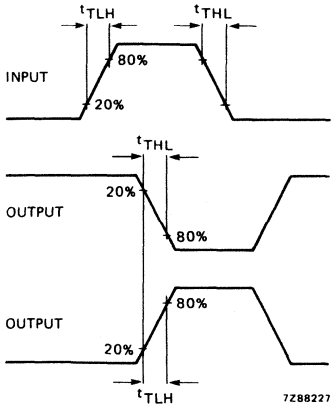


Fig. 5 Transition-times waveform (rise and fall times).

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	165	150	165	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	5,6,11,12	350	220	220	μA	
		9,10	390	245	245	μA	
		7	425	265	265	μA	
		13	460	290	290	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For output 14, pin 12 at V_{IHmax}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	pins 7,9 at V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For output 14, pins 7,9 at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For output 14, pin 12 at V_{IHC} pins 7,9 at V_{ILmin} (1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For output 14, pin 12 at V_{ILC} pins 7,9 at V_{ILmin} (1)

(1) Measure output after clock pulse appears at clock input (pin 13).

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remark
			−30	+25	+85		
Rise and fall propagation delay time							
C → Q	t_{PLH} / t_{PHL}	min.	0,8	1,0	1,4	ns	Clock to Output
		max.	4,8	4,5	5,0	ns	
C → $\overline{COUT}$	t_{PLH} / t_{PHL}	min.	2,0	2,5	2,4	ns	Clock → Carry out
		max	10,9	10,5	11,5	ns	
$\overline{CIN}$ → $\overline{COUT}$	t_{PLH} / t_{PHL}	min.	1,6	1,6	1,9	ns	Carry in → Carry out
		max.	7,4	6,9	7,5	ns	
Rise and fall transition time	t_{TLH} / t_{THL}	min.	0,9	1,0	1,0	ns	between 20% and 80%
		max.	3,3	3,3	3,5	ns	
Set-up time							
D → C	t_s	min.	3,5	3,5	3,5	ns	Fig. 6
S → C	t_s	min.	7,5	7,5	7,5	ns	
$\overline{CIN}$ → C	t_s	min.	4,5	3,7	4,5	ns	Fig. 7a
C → $\overline{CIN}$	t_s	min.	−1,0	−1,0	−1,0	ns	Fig. 7c
Hold time							
C → D	t_h	min.	0	0	0	ns	Fig. 6
C → S	t_h	min.	−2,5	−2,5	−2,5		
C → $\overline{CIN}$	t_h	min.	−1,6	−1,6	−1,6	ns	Fig. 7b
$\overline{CIN}$ → C	t_h	min.	4,0	3,1	4,0	ns	Fig. 7d
Counting frequency							
Count-up	$f_c$up	min.	125	125	125	MHz	
Count-down	$f_c$down	min.	125	125	125	MHz	

For **switching times test circuit** see Family Specifications.

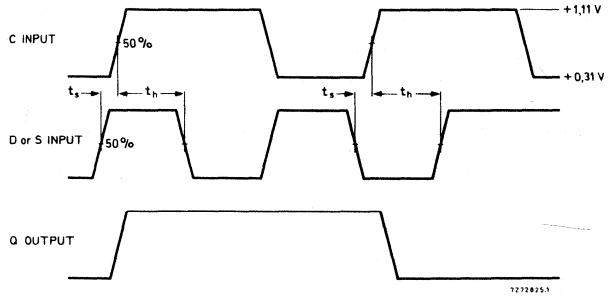


Fig. 6 Set-up and holding times waveform.

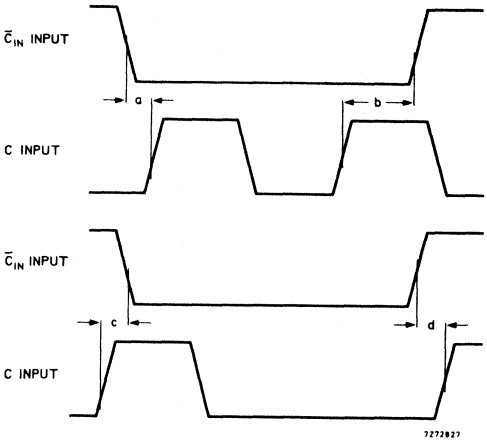


Fig. 7 Set-up and hold times waveform $\overline{C}_{IN} \longrightarrow C$.

(a) is the minimum time to wait to clock the counter after it has been enabled.

(b) is the minimum time that the counter may be clocked before it has been disabled.

(c) is the minimum time that a clock pulse may be applied with no effect on the state of the counter before it is enabled.

(d) is the minimum time to wait before a clock pulse may be applied with no effect on the state of the counter after it is disabled.

(b) and (c) may be negative numbers.

4-BIT UNIVERSAL SHIFT REGISTER

The 10141 is a four-bit serial-parallel-in, serial-parallel-out shift register. Inputs S_1 and S_2 are used to determine the four possible functions of the register, these being no shift, shift left, shift right and parallel entrance of data with no external gating of the clock. The other inputs DL and DR are intended for shifting in from the left and the right, while inputs D_0 to D_3 are normal data inputs. All four outputs are capable of driving 50 Ω lines.

When the register is operating for serial output only, the unused outputs must be tied low to V_{IL} or V_{EE}.

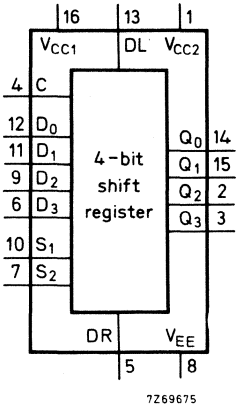


Fig. 1 Logic diagram.

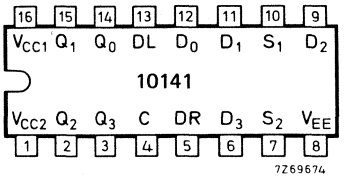


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Shift frequency	f_{shift}	typ.	200 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	425 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10141N: plastic 16-lead dual in-line (SOT-38).
10141F: ceramic 16-lead dual in-line (SOT-74).

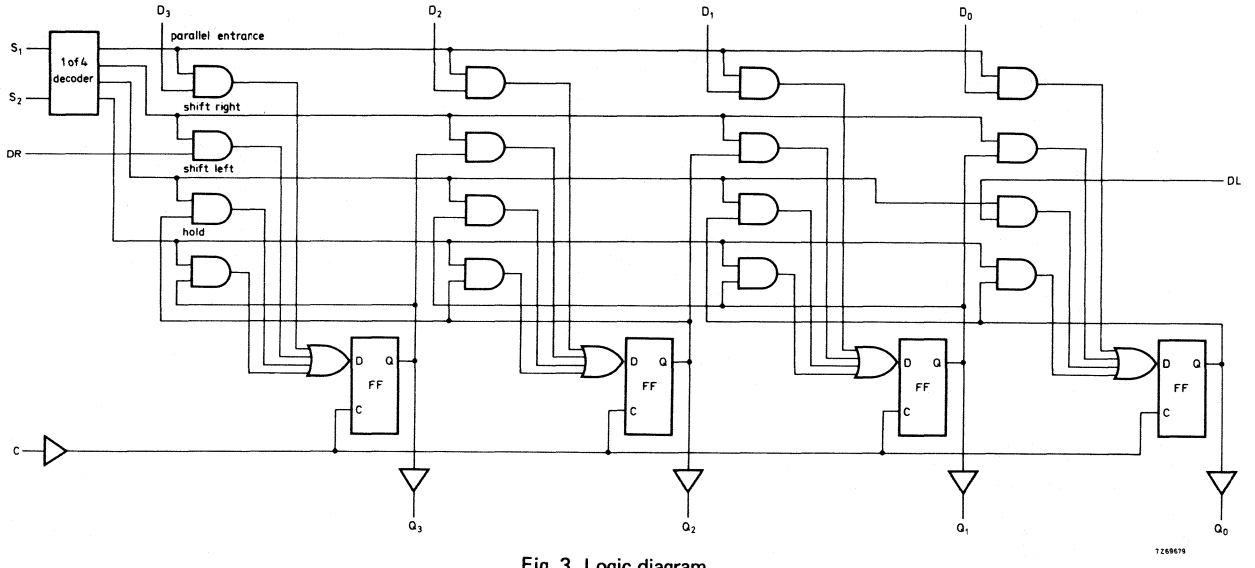


Fig. 3 Logic diagram.

FUNCTION TABLE

select inputs		operation mode	outputs			
S_1	S_2		$Q_{0(n+1)}$	$Q_{1(n+1)}$	$Q_{2(n+1)}$	$Q_{3(n+1)}$
L	L	parallel entrance	D_0	D_1	D_2	D_3
L	H	shift right*	Q_{1n}	Q_{2n}	Q_{3n}	DR
H	L	shift left*	DL	Q_{0m}	Q_{1n}	Q_{2n}
H	H	stop shift	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

* Outputs as they exist after pulse at "C" input with conditions as shown.

Pulse is positive transition of clock (C) input.

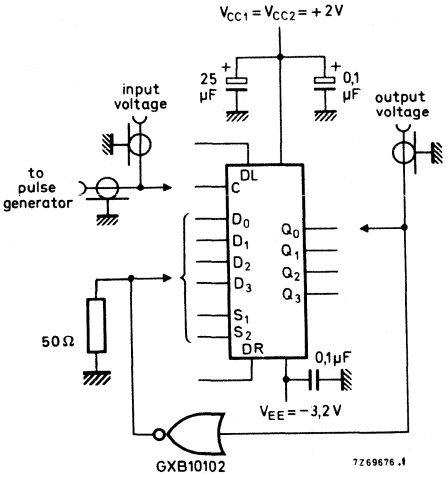


Fig. 4 Switching times test circuit.

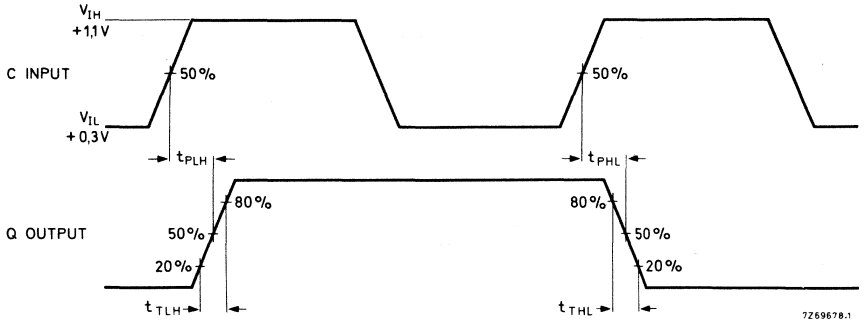


Fig. 5 Switching times waveforms.

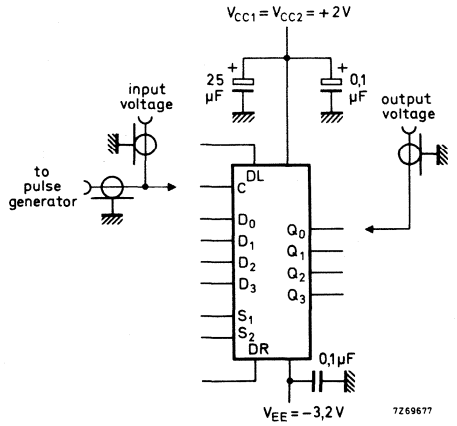


Fig. 6 Shift frequency test circuit.

Test procedure:

1. Set inputs D_1, D_2 and D_3 to LOW state (+0,3 V)
   D_0 to HIGH state (+1,1 V)
2. Apply clock pulse to C to set Q_0 in HIGH state.
3. Maintain clock input LOW.
   Set S_1 to LOW state (+0,3 V)
   S_2 to HIGH state (+1,1 V)
4. Test shift frequency.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	112	102	112	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test "Section"
Input current HIGH	I_{IHmax}	5,6,9,11,12,13	350	220	220	μA	
		7,10	390	245	245	μA	
		4	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

	symbol		pin under test	T_{amb} (°C)			unit	conditions	
				−30	+25	+85		pin	test voltage
Output voltage HIGH	V_{OH}	min.	3	−1 060	− 960	− 890	mV	6	V_{IHmax}
		typ.			− 880		mV	4	V_{IH}
		max.		− 890	− 810	− 700	mV		
Output voltage LOW	V_{OL}	min.	3	−1 890	−1 850	−1 825	mV		
		typ.			−1 720		mV	4	V_{IH}
		max.		−1 675	−1 650	−1 615	mV		
Output threshold voltage HIGH (1)	V_{OHT}	min	3	−1 080	− 980	− 910	mV	6	V_{IHT}
								4	V_{IH}
								4	V_{IHmax} (2)
								7	V_{ILT}
								4	V_{IH}
								6	V_{IHmax} (2)
								4	V_{IH}
Output threshold voltage LOW (1)	V_{OLT}	max	3	−1 655	−1 630	−1 595	mV	4	V_{ILT}
								6	V_{ILT}
								4	V_{IH}
								7	V_{ILT} (3)
								4	V_{IH}
								4	V_{IHT} (3)
								6	V_{IHmax}
								4	V_{ILT}

(1): These tests to be performed in sequence as shown.
(2): Reset to zero before performing test.
(3): Reset to HIGH state (1) before performing test.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay rise and fall times	t_{PLH} / t_{PHL}	min.	1,7	1,8	2,0	ns	
		max.	3,9	3,8	4,2	ns	
Transition rise and and fall times	t_{TLH} / t_{THL}	min.	1,0	1,1	1,1	ns	
		max.	3,4	3,3	3,6	ns	
Set-up time							
$D \rightarrow C$	t_{DCS}	min.	2,5	2,5	2,5	ns	see Fig. 4 and 5
$S_n \rightarrow C$	t_{SSC}	min.	5,5	5,0	5,5	ns	
Hold time							
$C \rightarrow D$	t_{CHD}	min.	1,5	1,5	1,5	ns	
$C \rightarrow S_n$	t_{CHS}	min.	1,5	1,5	1,5	ns	
Shift frequency	f_{shift}	min.	150	150	150	MHz	see Fig. 6

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-TO-1 MULTIPLEXER

The 10158 is a high speed, low power, quadruple 2-to-1 multiplexer. With respect to a single control signal it transmits to a common output pin the data present on either of two input pins. As contrasted with the 10159 the 10158 has no enable input and non-inverting outputs. It includes high-impedance input pull-down resistors and open emitter outputs.

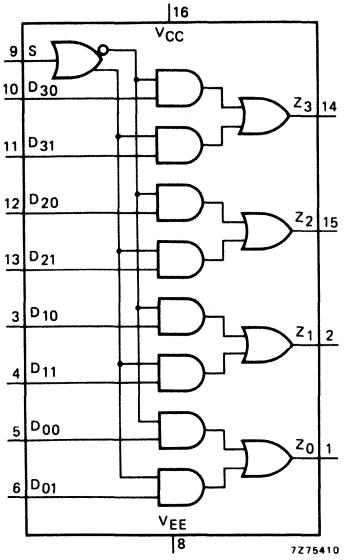


Fig. 1 Logic diagram.

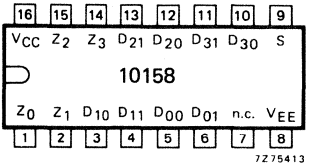


Fig. 2 Pin designation.

V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay: data to output	t_{PLH}	typ.	2,2 ns
select to output	t_{PLH}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	162 mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10158N: plastic 16-lead dual in-line (SOT-38).
10158F: ceramic 16-lead dual in-line (SOT-74).

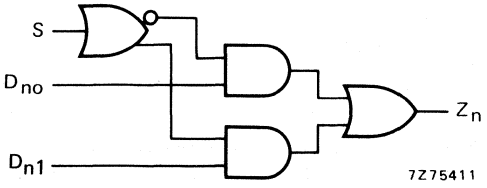


Fig. 3 Logic function (one multiplexer).

FUNCTION TABLE

inputs			output
D_{no}	D_{n1}	S	Z_n
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

Positive logic

H = HIGH state
(the more positive voltage) = 1

L = LOW state
(the less positive voltage) = 0

X = state is immaterial

RATINGS see Family Specifications

For **switching times test circuit** and **waveform** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	53	48	53	mA	see "How to test section
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	
Input current HIGH	I_{IHmax}	9*	360	225	225	μA	
		other inputs	400	250	250	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	S at V_{IL}
		typ.		− 880		mV	One data at
		max.	− 890	− 810	− 700	mV	V_{IHmax}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Inputs at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation D → Q delay times	t_{PLH}/ t_{PHL}	min.	1,3	1,2	1,3	ns	Data to output
		max.	3,1	3,0	3,2	ns	
S → Q		min.	2,5	2,4	2,5	ns	Select to output
		max.	4,8	4,5	4,8	ns	
Transition times rise and fall	t_{TLH}/	min.	1,6	1,5	1,6	ns	20% to 80%
		max.	3,4	3,3	3,4	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

QUADRUPLE 2-TO-1 MULTIPLEXER

The 10159 is a high speed, low power, quadruple 2-to-1 multiplexer. With respect to a single control signal it transmits to a common output pin the data present on either of two input pins. As contrasted with the 10158 the 10159 has a common enable input and inverting outputs. It includes high-impedance input pull-down resistors and open emitter outputs.

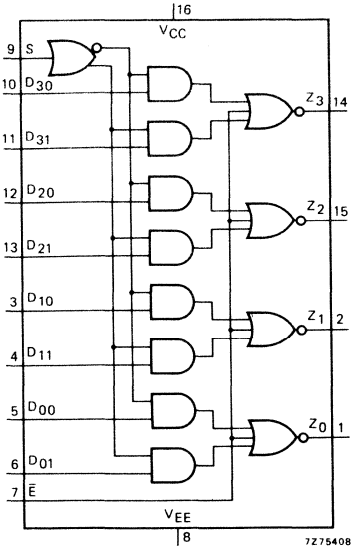


Fig. 1 Logic diagram.

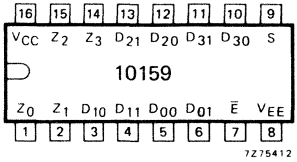


Fig. 2 Pin designation.

V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay: data to output	t_{PLH}	typ.	2,2 ns
select to output	t_{PLH}	typ.	3,3 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	162 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10159N: plastic 16-lead dual in-line (SOT-38).
10159F: ceramic 16-lead dual in-line (SOT-74).

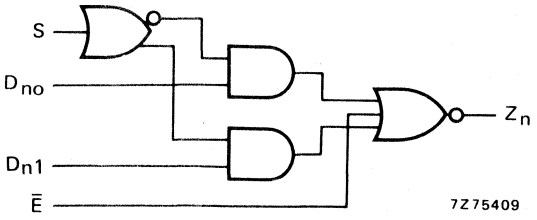


Fig. 3 Logic diagram (one multiplexer).

FUNCTION TABLE

inputs				output
D_{no}	D_{n1}	S	$\bar{E}$	Z_n
X	X	X	H	L
L	X	L	L	H
H	X	L	L	L
X	L	H	L	H
X	H	H	L	L

Positive logic

H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the less positive voltage) = 0
X = state is immaterial

RATINGS see Family Specifications

For **switching times test circuit** and **waveforms** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	58	53	58	mA	
Input current LOW	I_{ILmin}	3*	0.5	0.5	0.3	μA	see "How to test section
Input current HIGH	I_{IHmax}	9*	360	225	225	μA	
		other inputs	400	250	250	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Inputs at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	S and E at V_{ILmin}
		typ.		−1 720		mV	One input at
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation D → Q delay times	t_{PLH}/ t_{PHL}	min.	1,1	1,2	1,1	ns	Data to output
		max.	3,8	3,3	3,8	ns	
S → Q		min.	1,5	1,5	1,5	ns	Select to output
		max.	5,3	5,0	5,3	ns	
$\overline{E}$ → Q		min.	1,4	1,5	1,4	ns	Enable to output
		max.	5,3	5,0	5,3	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,0	ns	20% to 80%
		max.	5,0	4,5	5,0	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

12-BIT PARITY CHECKER/GENERATOR

The 10160 is a 12-bit parity checker or generator. The output goes HIGH when an odd number of inputs are HIGH. If parity detection or generation is required for less than 12 bits.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

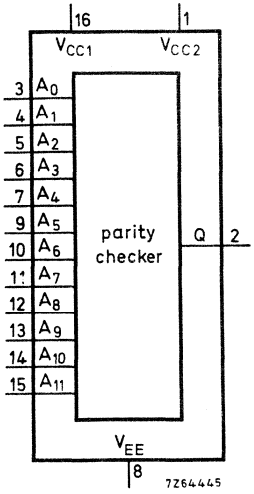


Fig. 1 Logic diagram.

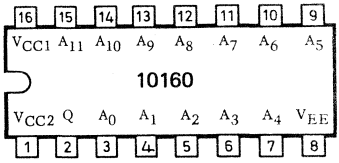


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 4,5	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_D	typ. 310	mW

For **FAMILY DATA** see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10160N: plastic 16-lead dual in-line (SOT-38).
10160F: ceramic 16-lead dual in-line (SOT-74).

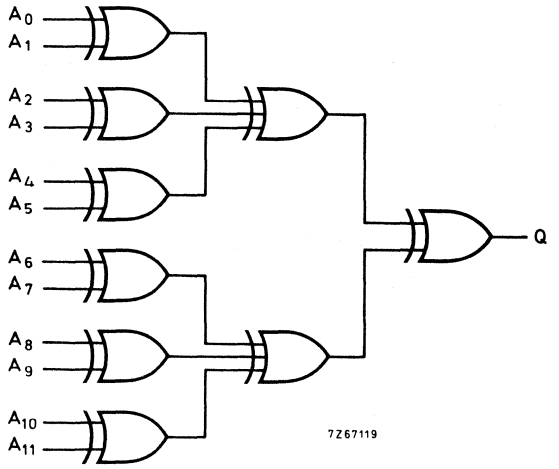


Fig. 3 Logic function.

FUNCTION TABLE

sum of inputs at HIGH state	Q
odd	H
even	L

positive logic:

HIGH state = 1
LOW state = 0

$$Q = A_0 \oplus A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus A_6 \oplus A_7 \oplus A_8 \oplus A_9 \oplus A_{10} \oplus A_{11}.$$

RATINGS see Family Specifications.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2{,}0$ V; $V_{EE} = -3{,}2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/t_{PHL}	min.	1,8	2,0	2.0	ns	
		typ.		4,5		ns	50% to 50%
		max.	8,1	7,5	8,0	ns	
Transition times rise and fall	t_{TLH}/t_{THL}	min.	1,1	1,1	1,0	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,5	3,3	3,5	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	86	78	86	mA	
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	3,6,7,11,12,15	425	265	265	μA	
		4,5,9.10,13,14	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Odd number of inputs at V_{IHmax}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	Other inputs at V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Even number of inputs at V_{IHmax}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	Other inputs at V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC} Other inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC} Other inputs at V_{ILmin}

For **switching times test circuit** and **waveform** see Family Specifications.

THREE-BIT DECODER

one of eight lines LOW

The 10161 is a three-bit decoder with two enable inputs.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

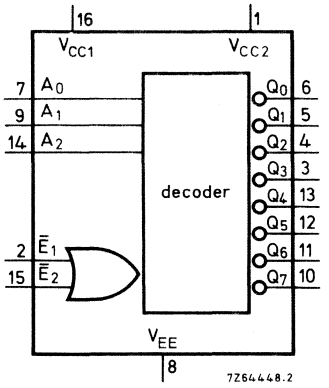


Fig. 1 Logic diagram.

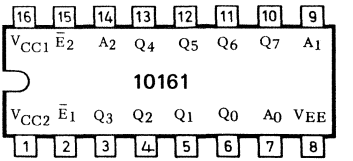


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	330 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10161N: plastic 16-lead dual in-line (SOT-38).
10161F: ceramic 16-lead dual in-line (SOT-74).

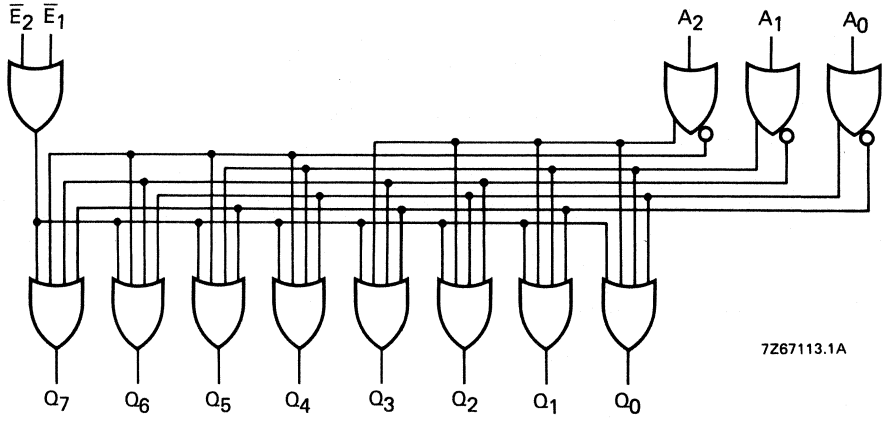


Fig. 3 Logic function.

A_0 to A_2: binary inputs; $\overline{E}_1$; $\overline{E}_2$: enable inputs; Q_0 to Q_7: decoded outputs.

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	H	H	H	H	H	H	H	H
L	H	X	X	X	H	H	H	H	H	H	H	H
H	L	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L

positive logic: H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

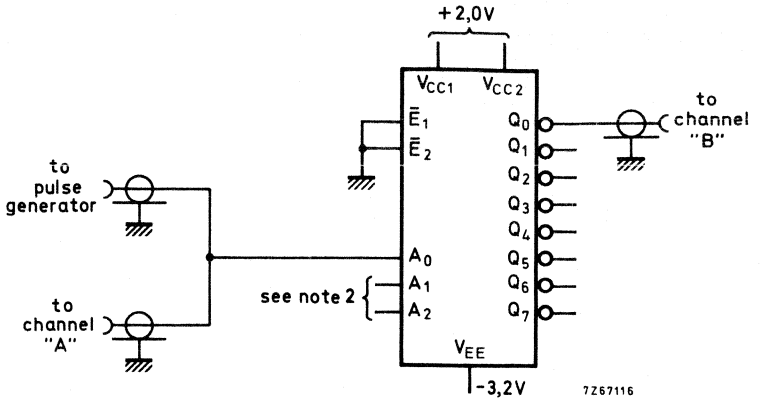


Fig. 4 Switching times test circuit.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	84	76	84	mA	
Input current LOW	I_{ILmin}	2*	0,5	0,5	0,3	μA	see "How to test section
Input current HIGH	I_{IHmax}	2*	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For each output Pin 2 or 15 at V_{IHmax} or pin 15 or 2 at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For output 10 All inputs at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For each output Pin 2 or 15 at V_{IHC}, 15 or 2 at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For output 11 Pin 7 at V_{IHC} Pins 9, 14 at V_{ILmin} For output 5 Pin 7 at V_{ILC} Pins 9, 14 at V_{IHmax}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,5	1,5	1,5	ns	50% to 50%
		typ.		4,0		ns	
		max.	6,2	6,0	6,4	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	20% to 80%
		typ.		2,0		ns	
		max.	3,3	3,3	3,5	ns	

For **switching times waveforms** see Family Specifications.

THREE-BIT DECODER

one of eight lines HIGH

The 10162 is a three-bit decoder with two enable inputs.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

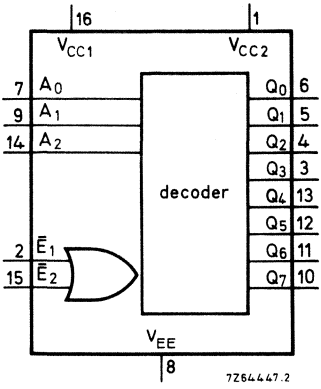


Fig. 1 Logic diagram.

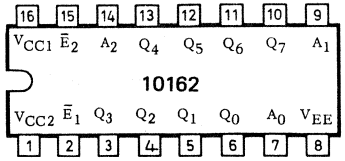


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	330 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10162N: plastic 16-lead dual in-line (SOT-38).
10162F: ceramic 16-lead dual in-line (SOT-74).

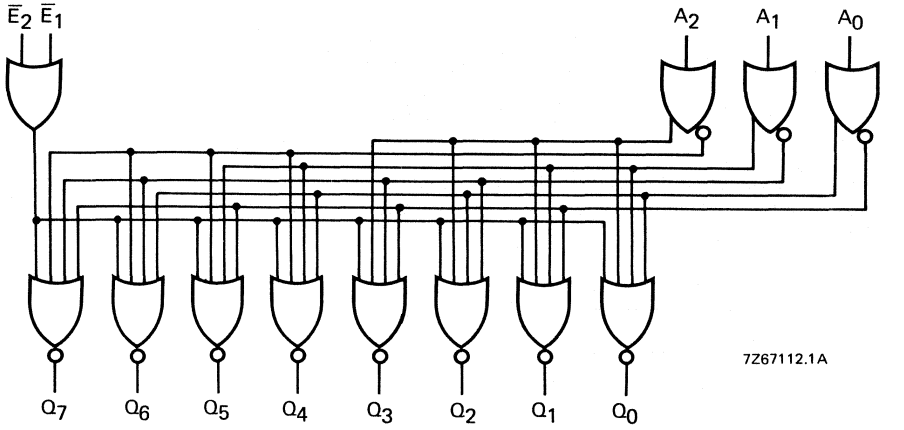


Fig. 3 Logic function.

A_0 to A_2: binary inputs; $\overline{E}_1$; $\overline{E}_2$: enable inputs; Q_0 to Q_7: decoded outputs.

FUNCTION TABLE

enable inputs		binary inputs			decimal outputs							
$\overline{E}_1$	$\overline{E}_2$	A_0	A_1	A_3	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	H	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	L	L	L	L	L	L	L	L
H	L	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	L	H	H	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

positive logic: H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

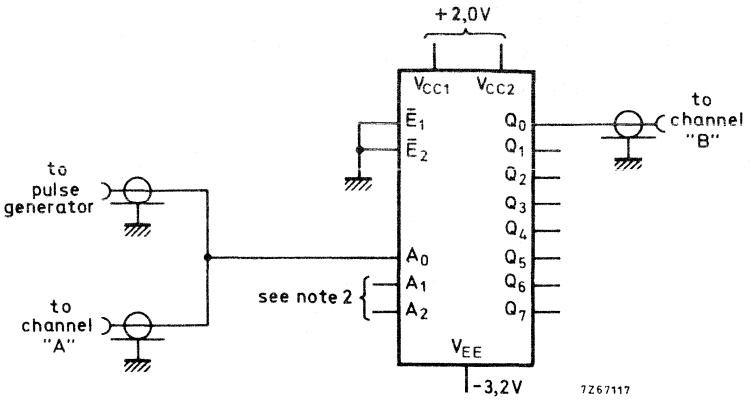


Fig. 4 Switching times test circuit.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	84	76	84	mA	
Input current LOW	I_{ILmin}	2*	0,5	0,5	0,3	μA	see "How to test section
Input current HIGH	I_{IHmax}	2*	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For output 10
		typ.		− 880		mV	All inputs at
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For each output
		typ.		−1 720		mV	2 or 15 at V_{IHmax}
		max.	−1 675	−1 650	−1 615	mV	15 or 2 at V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For output 11 Pin 7 at V_{IHC} Pins 9, 14 at V_{ILmin} For output 5 Pin 7 at V_{ILC} Pins 9,14 at V_{IHmax}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For each output Pin 2 or 15 at V_{IHC} Pins 15 or 2 at V_{ILmin}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,5	1,5	1,5	ns	
		typ.		4,0		ns	50% to 50%
		max.	6,2	6,0	6,4	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,3	3,3	3,5	ns	

For **switching times waveforms** see Family Specifications.

EIGHT-INPUT MULTIPLEXER

The 10164 performs 8 input multiplexing with enable input. The output goes LOW when not
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

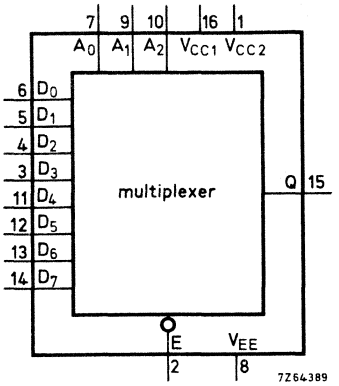


Fig. 1 Logic diagram.

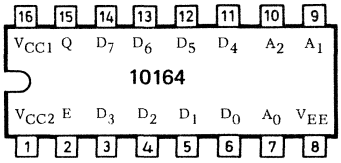


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Average propagation delay	t_{PLH}	typ. 3	ns
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_D	typ. 310	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10164N: plastic 16-lead dual in-line (SOT-38).
10164F: ceramic 16-lead dual in-line (SOT-74).

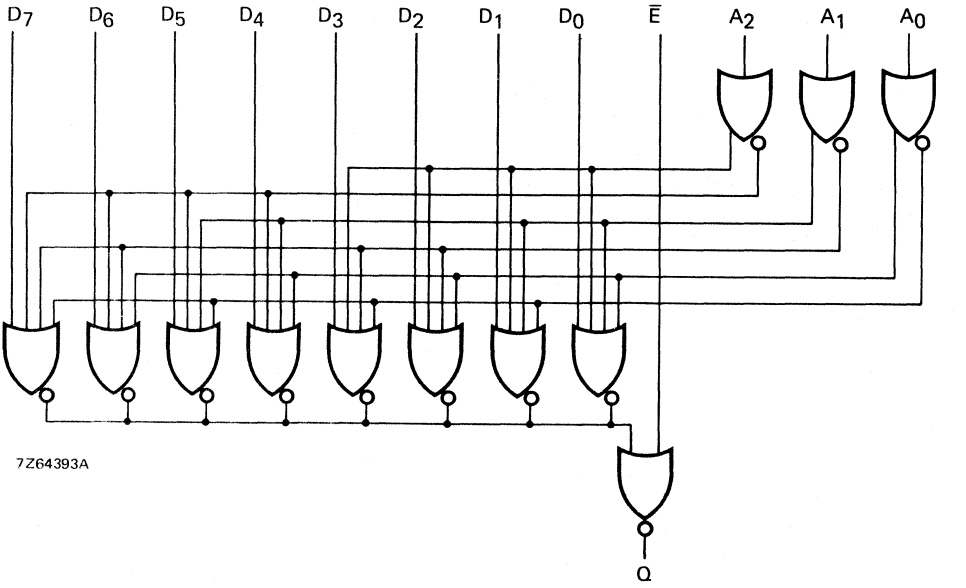


Fig. 3 Logic function.

A_0 to A_2 = address inputs; D_0 to D_7 = data inputs; $\overline{E}$ = enable input.

inputs												output
A_0	A_1	A_2	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

Function table

H = HIGH state (the more positive voltage); L = LOW state (the less positive voltage); X = state is immateria

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	83	75	83	mA	
Input current LOW	I_{ILmin}	2*	0,5	0,5	0,3	μA	see "How to test section
Input current HIGH	I_{IHmax}	2*	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	D_0 at V_{IHmax}
		typ.		− 880		mV	Other inputs at
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	$\overline{E}$ at V_{IHmax}
		typ.		−1 720		mV	Other inputs at
		max.	−1 675	−1 650	−1 615	mV	V_{IL}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	D_0 at V_{IHC} Other inputs at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	$\overline{E}$ at V_{IHC} Other inputs at V_{ILC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
$D_n \rightarrow Q$	t_{PLH}/ t_{PHL}	min.	1,5	1,5	1,6	ns	
		max.	4,7	4,5	4,8	ns	
$A_n \rightarrow Q$		min.	1,9	2,0	2,2	ns	50% to 50%
		max.	6,3	6,0	6,5	ns	
$\overline{E} \rightarrow Q$		min.	0,9	1,0	1,0	ns	
		max.	3,3	2,9	3,1	ns	
Transition rise and fall time	t_{THL}/ t_{TLH}	min.	0,9	1,1	1,2	ns	20% to 80%
		max.	3,3	3,3	3,6	ns	

For **switching times waveforms** see Family Specifications.

8-INPUT PRIORITY ENCODER

The 10165 is able to encode eight inputs to binary coded outputs. Each output is stored in a D-type latch which allows synchronous operation. When the clock input is LOW the outputs follow the inputs and latch when the clock goes HIGH. The output code is that of the highest order input so that any input of lower priority is ignored.

The input is active when HIGH (e.g. the three binary outputs are LOW when input D_0 is HIGH). Output Q_3 is HIGH when any input is HIGH, which allows direct extension into another priority encoder when more than 8 inputs are used.

The device can be used in many applications, such as testing systems and checking system status in control processors and peripheral controllers. It can also be used to generate binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.
All unused inputs must be tied LOW to V_{IL} or V_{EE}.

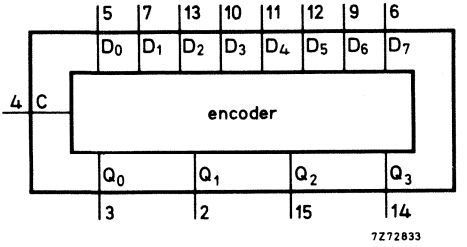


Fig. 1 Block diagram.

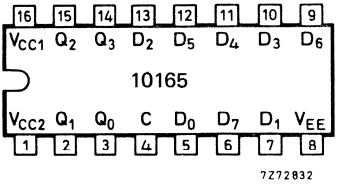


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature	T_{amb}		−30 to + 85 °C
Average propagation delay with data inputs	t_{PLH}	typ.	5,5 ns
Average propagation delay with clock inputs	t_{PLH}	typ.	3,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	545 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10165N: plastic 16-lead dual in-line (SOT-38).
10165F: ceramic 16-lead dual in-line (SOT-74).

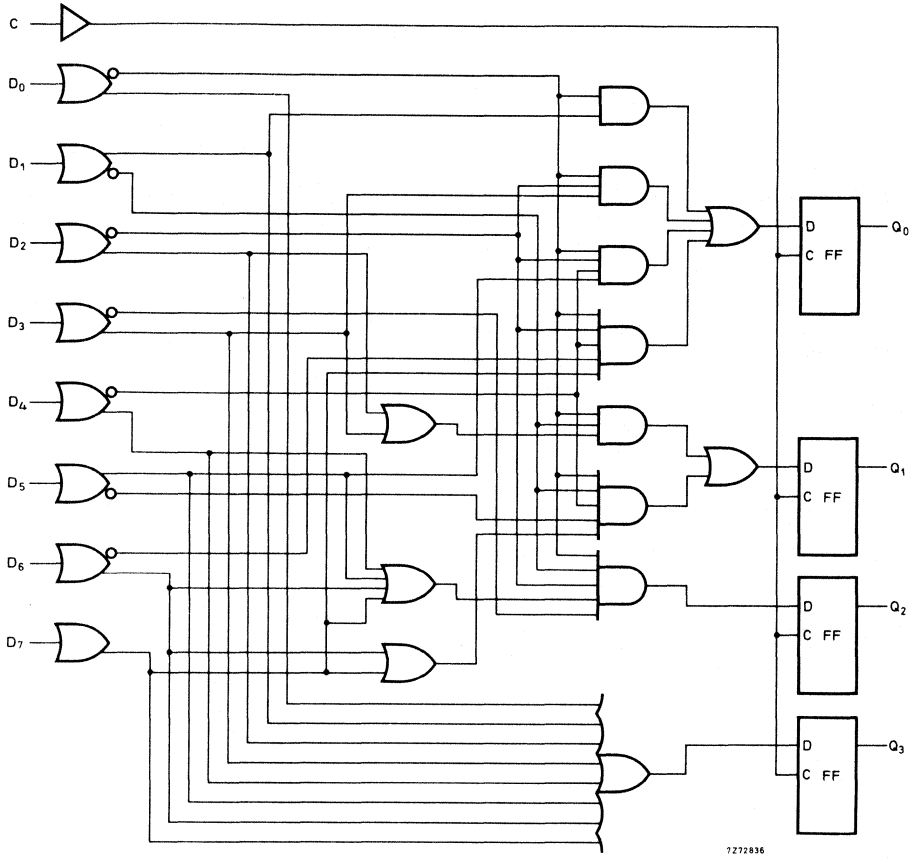


Fig. 3 Logic function.

FUNCTION TABLE

inputs								outputs			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_3	Q_2	Q_1	Q_0
H	X	X	X	X	X	X	X	H	L	L	L
L	H	X	X	X	X	X	X	H	L	L	H
L	L	H	X	X	X	X	X	H	L	H	L
L	L	L	H	X	X	X	X	H	L	H	H
L	L	L	L	H	X	X	X	H	H	L	L
L	L	L	L	L	H	X	X	H	H	L	H
L	L	L	L	L	L	H	X	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	144	131	144	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	4	390	245	245	μA	
		other inputs	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax} on Data V_{ILmin} on clock
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin} on Clock input
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} on Data V_{ILmin} on clock
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on Data V_{ILmin} on clock

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
D → Q	t_{PLH}/ t_{PHL}	min.	2,0	2,0	2,0	ns	
		max.	7,0	7,0	8,0	ns	
C → Q		min.	1,5	1,5	1,5	ns	
		max.	4,5	4,0	4,5	ns	
Transition rise and fall time	t_{THL}/ t_{TLH}	min.	1,1	1,1	1,1	ns	20% to 80%
		max.	3,5	3,3	3,5	ns	
Set-up time	t_s	min.	6,0	6,0	6,0	ns	D → C
Hold time	t_h	min.	1,0	1,0	1,0	ns	

For **switching times waveforms** see Family Specifications.

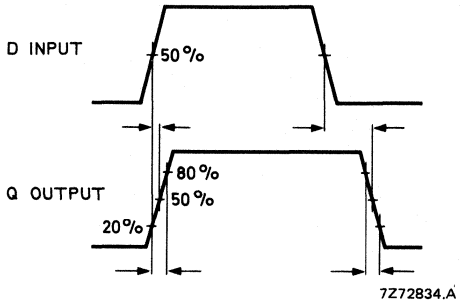


Fig. 4 Switching times waveforms **data** to output.

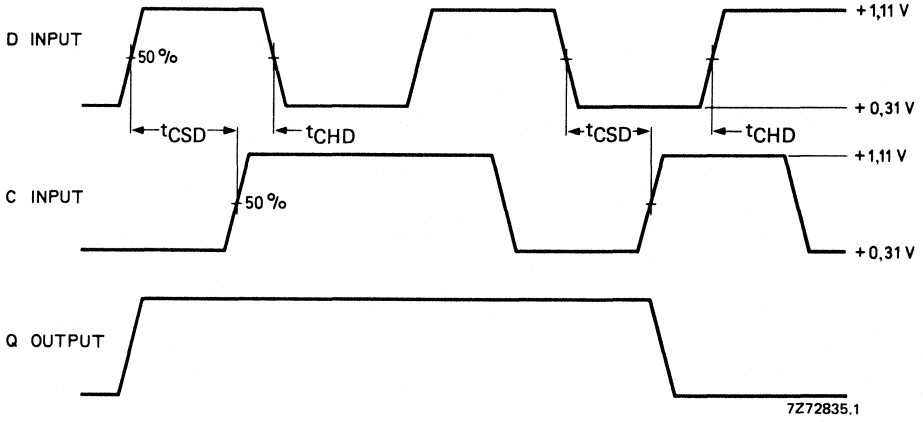


Fig. 5 Switching times waveforms; set-up and hold times DATA to CLOCK.

Notes

1. Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be present at the data input (D).
2. Hold-times are the minimum times after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

DUAL TWO-BIT DECODER
one of four lines LOW

The 10171 is a dual two-bit decoder with one common and two individual enable inputs. The common enable ($\overline{E}$), when HIGH, forces all outputs HIGH.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

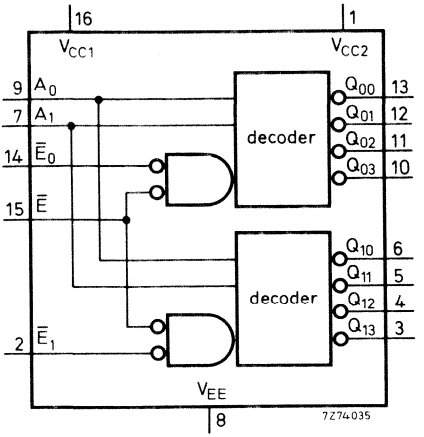


Fig. 1 Logic diagram.

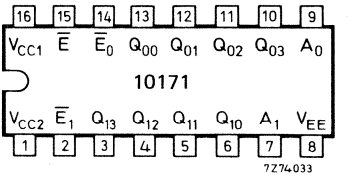


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	325 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10171N: plastic 16-lead dual in-line (SOT-38).
10171F: ceramic 16-lead dual in-line (SOT-74).

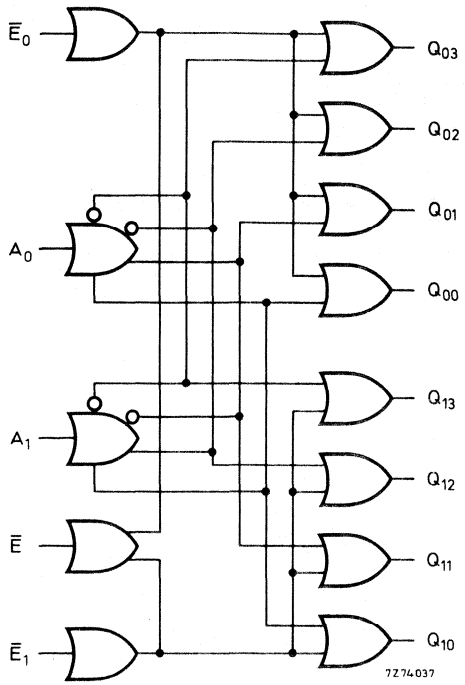


Fig. 3 Logic diagram.

LOGIC FUNCTIONS

$Q_{00} = \overline{E} + \overline{E_0} + A_0 + A_1$
$Q_{01} = \overline{E} + \overline{E_0} + A_0 + \overline{A_1}$
$Q_{02} = \overline{E} + \overline{E_0} + \overline{A_0} + A_1$
$Q_{03} = \overline{E} + \overline{E_0} + \overline{A_0} + \overline{A_1}$

$Q_{10} = \overline{E} + \overline{E_1} + A_0 + A_1$
$Q_{11} = \overline{E} + \overline{E_1} + A_0 + \overline{A_1}$
$Q_{12} = \overline{E} + \overline{E_1} + \overline{A_0} + A_1$
$Q_{13} = \overline{E} + \overline{E_1} + \overline{A_0} + \overline{A_1}$

FUNCTION TABLE

enable inputs			inputs		outputs							
$\overline{E}$	$\overline{E_0}$	$\overline{E_1}$	A_0	A_1	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{03}
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	85	77	85	mA	
Input current LOW	I_{ILmin}	2*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	2*	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax} on Pin 15 for outputs 6,13
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin} on inputs for outputs 6,13
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} on Pin 15 for outputs 6,13
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on Pin 15 for outputs 6,13

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,5	1,5	1,5	ns	
		typ.		4,0		ns	50% to 50%
		max.	6,2	6,0	6,4	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,3	3,3	3,4	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL TWO-BIT DECODER

one of four lines HIGH

The 10172 is a dual two-bit decoder with one common and two individual enable inputs. The common enable (E), when HIGH, forces all outputs LOW.

Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

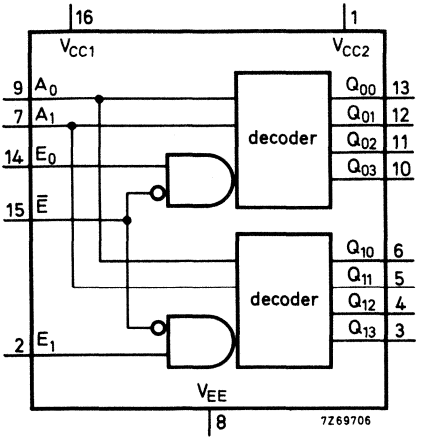


Fig. 1 Logic diagram.

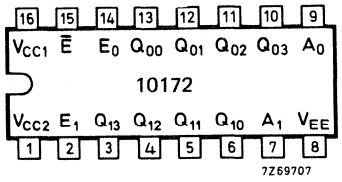


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	4,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	325 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINE (see Package Outlines)

10172N: plastic 16-lead dual in-line (SOT-38).
10172F: ceramic 16-lead dual in-line (SOT-74).

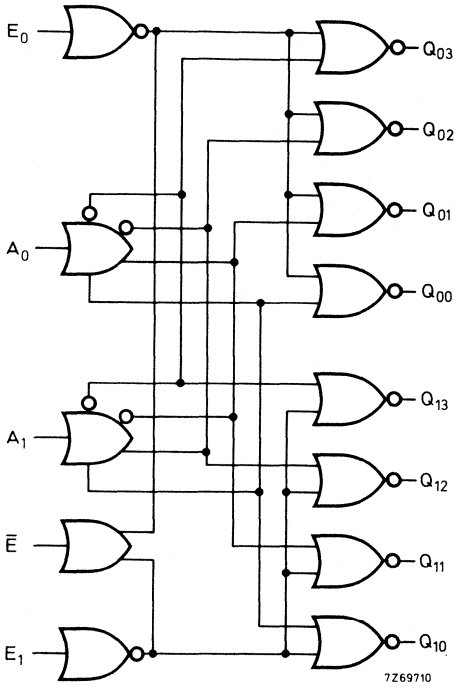


Fig. 3 Logic function.

LOGIC FUNCTIONS

$$Q_{00} = \overline{\overline{E} + \overline{E_0} + A_0 + A_1}$$
$$Q_{01} = \overline{\overline{E} + \overline{E_0} + A_0 + \overline{A_1}}$$
$$Q_{02} = \overline{\overline{E} + \overline{E_0} + \overline{A_0} + A_1}$$
$$Q_{03} = \overline{\overline{E} + \overline{E_0} + \overline{A_0} + \overline{A_1}}$$
$$Q_{10} = \overline{\overline{E} + \overline{E_1} + A_0 + A_1}$$
$$Q_{11} = \overline{\overline{E} + \overline{E_1} + A_0 + \overline{A_1}}$$
$$Q_{12} = \overline{\overline{E} + \overline{E_1} + \overline{A_0} + A_1}$$
$$Q_{13} = \overline{\overline{E} + \overline{E_1} + \overline{A_0} + \overline{A_1}}$$

FUNCTION TABLE

enable inputs			inputs		outputs							
$\overline{E}$	E_1	E_0	A_0	A_1	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{01}
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	L	L	L	L	H	L	L	L
H	X	X	X	X	L	L	L	L	L	L	L	L

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

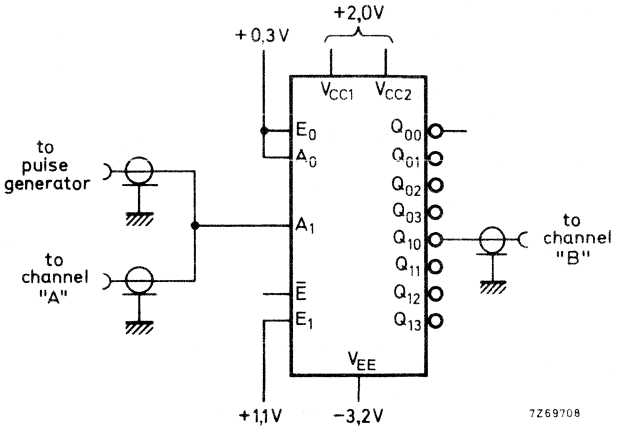


Fig. 4 Switching times test circuit.

For **switching times waveform** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	85	77	85	mA	
Input current LOW	I_{ILmin}	2*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	2*	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_{IHmax} on pins 2, 14 for outputs 6, 13
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_{ILmin} on pins 2,14 for outputs 6,13
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_{IHC} on pins 2,14 for outputs 6,13
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_{ILC} on pins 2,14 for outputs 6,13

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,5	1,5	1,5	ns	
		typ.		4,0		ns	50% to 50%
		max.	6,2	6,0	6,4	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	
		typ.		2,0		ns	20% to 80%
		max.	3,3	3,3	3,4	ns	

For switching times waveform see Family Specifications.

QUADRUPLE MULTIPLEXER

The 10173 is a quadruple 2-input multiplexer with latched outputs. Each multiplexer has two inputs, selected by the common data select input (D_S). Outputs are latched when the clock is HIGH.
All unused inputs must be tied LOW to V_{IL} or V_{EE}.

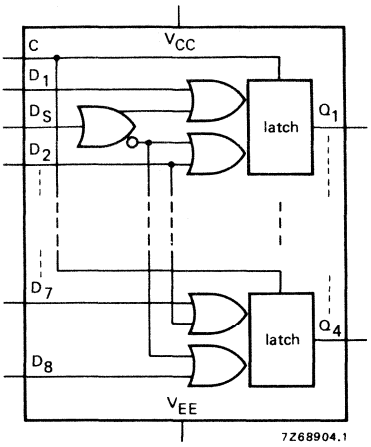


Fig. 1 Logic diagram.

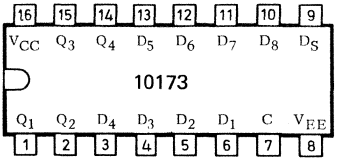


Fig. 2 Pin designation.
$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	2,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	275 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10173N: plastic 16-lead dual in-line (SOT-38).
10173F: ceramic 16-lead dual in-line (SOT-74).

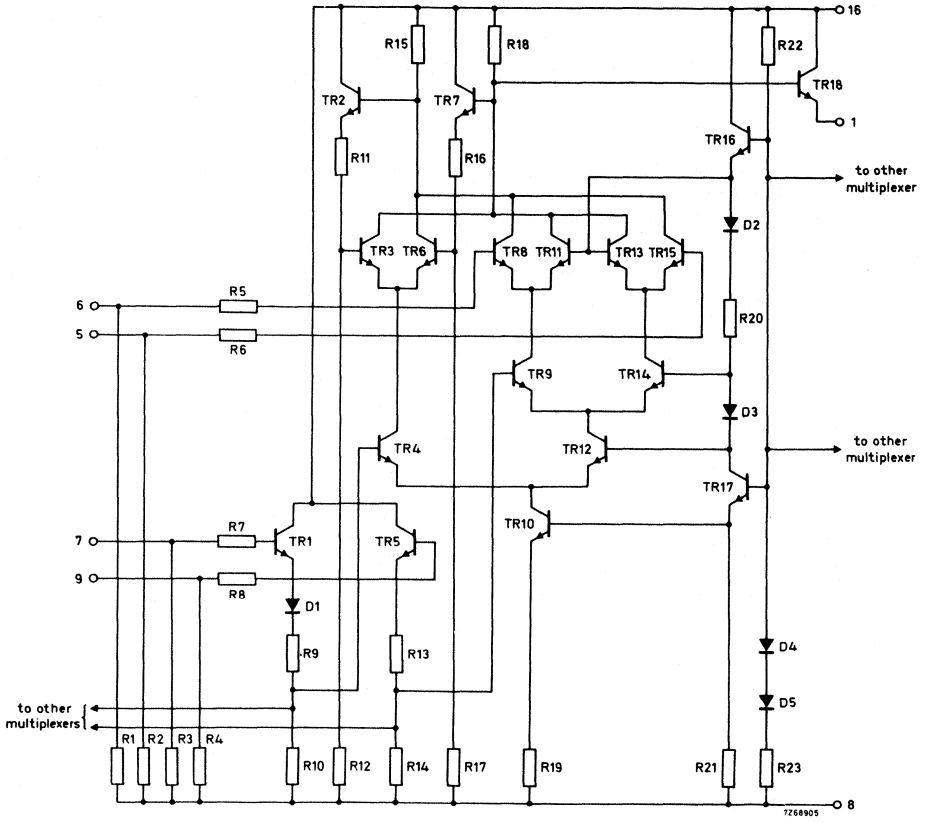


Fig. 3 Circuit diagram (one multiplexer).

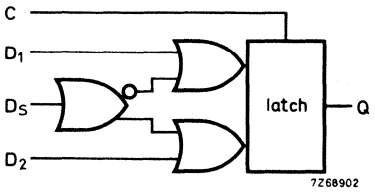


Fig. 4 Logic function.

FUNCTION TABLE

D_S	C	Q_{n+1}
H	L	D_1
L	L	D_2
X	H	Q_n

Positive logic: HIGH state = 1
LOW state = 0
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS see Family Specifications.

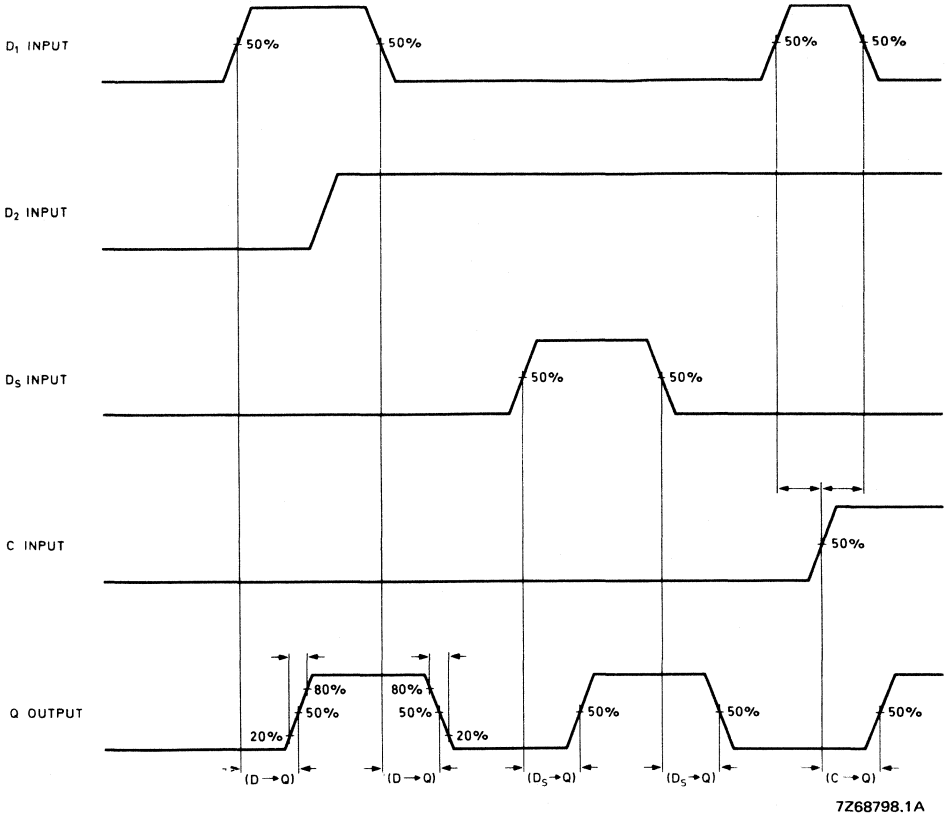


Fig. 5 Switching times waveforms.

Conditions for input signal: $t_r = t_f = 2{,}0$ ns (20% to 80%); $V_{IH} = +1{,}11$ V; $V_{IL} = +0{,}31$ V.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+95		
Supply current	I_{EEmax}	8	73	66	73	mA	
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	see "How to test section
Input current HIGH	I_{IHmax}	7,9	400	250	250	μA	
		3,4,5,6,10,11	470	295	295	μA	
		12,13	470	295	295	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Data at V_{IHmax}
		typ.		− 880		mV	C and D_S
		max.	− 890	− 810	− 700	mV	at V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Data, C and D_S
		typ.		−1 720		mV	at V_{ILmin}
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	Data at V_{IHC} C, D_S at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	Data, C and D_S at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise and fall propagation delay times	$\overline{t_{PLH}}$ / $\overline{t_{PHL}}$						
D → Q		min.	0,8	1,0	1,1	ns	Data
		max.	3,7	3,5	5,3	ns	
C → Q		min.	1,6	1,6	1,4	ns	Clock
		max.	7,2	6,8	6,8	ns	
D_S → Q		min.	1,1	1,3	1,2	ns	Select
		max.	6,2	5,7	6,7	ns	
Rise and fall transition time	$\overline{t_{TLH}}$ / $\overline{t_{THL}}$	min.	1,2	1,5	1,4	ns	between 20% and 80%
		max	4,0	3,5	4,0	ns	
Rise time clock drive	t_{TLH}	min.	1,2	1,5	1,4	ns	between 20% and 80%
		max.	5,0	4,5	5,0	ns	
Set-up time							
D → C	t_{DSC}	min	2,0	2,0	2,0	ns	
D_S → C	t_{DSSC}	min.	3,0	3,0	3,0	ns	
Hold time							
C → D	t_{CHD}	min.	2,5	2,5	2,5	ns	
C → D_S	t_{CHDS}	min.	1,5	1,5	1,5	ns	

For **switching times test circuit** see Family Specifications.

DUAL 4 TO 1 MULTIPLEXER

The 10174 performs two 4-input multiplexer functions. The output of each multiplexer reflects one of the 4 data inputs determinated by the states on the two select inputs. An enable input is provided for easy bit expansion by wire-ORing several multiplexers. Each output will go LOW with the enable input in the HIGH state. Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

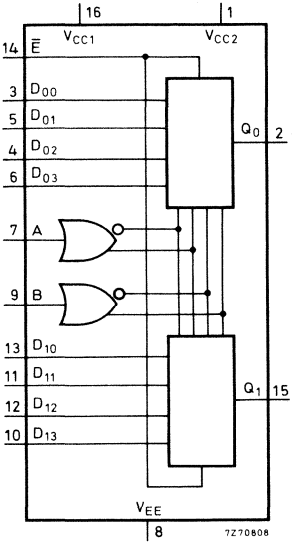


Fig. 1 Logic diagram.

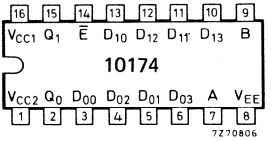


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

A, B: select inputs
D_{00} to D_{03}: data inputs for Q_0
D_{10} to D_{13}: data inputs for Q_1
$\bar{E}$: enable input

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−3,0 to + 85 °C
Average propagation delay	t_{PLH}	typ.	3,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	310 mW

PACKAGE OUTLINES (see Package Outlines).

10174N: plastic 16-lead dual in-line (SOT-38).
10174F: ceramic 16-lead dual in-line (SOT-74).

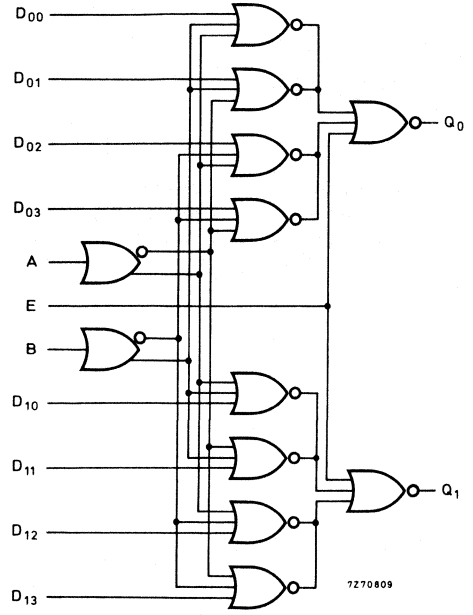


Fig. 3 Logic function.

FUNCTION TABLE

inputs			outputs	
A	B	$\overline{E}$	Q_0	Q_1
L	L	L	D_{00}	D_{10}
L	H	L	D_{02}	D_{12}
H	L	L	D_{01}	D_{11}
H	H	L	D_{03}	D_{13}
X	X	H	L	L

Positive logic:

H = HIGH state
(the more positive voltage) = 1
L = LOW state
(the less positive voltage) = 0
X = state is immaterial

FAMILY DATA and **RATINGS** see Family Specifications.

For **switching times waveforms** see Family Specifications

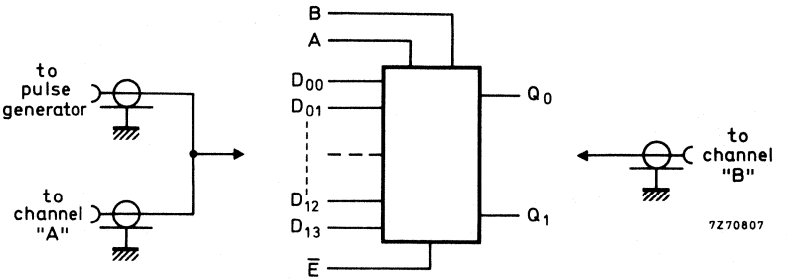


Fig. 4 Switching times test circuit.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	80	73	80	mA	
Input current LOW	I_{ILmin}	3*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	14	525	310	330	μA	
		other pins	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For output 2
		typ.		− 880		mV	pin 3 at V_{IHmax}
		max.	− 890	− 810	− 700	mV	(See note 1)
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For output 2
		typ.		−1 720		mV	pin 14 at V_{IHmax}
		max.	−1 675	−1 650	−1 615	mV	(See note 1)
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For output 2 pin 13 at V_{IHC} (See note 1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For output 2 pin 14 at V_{ILC} (See note 1)

Note 1: Non-specified input pins should be connected to V_{ILmin}.

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
D → Q	t_{PLH}/ t_{PHL}	min.	1,4	1,5	1,4	ns	
		max.	4,8	4,5	4,8	ns	
A;B → Q		min.	1,9	2,0	2,1	ns	50% to 50%
		max.	6,4	6,0	6,4	ns	
$\overline{E}$ → Q		min.	1,0	1,0	0,9	ns	
		max.	3,1	2,9	3,2	ns	
Transition rise and fall time	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	20% to 80%
		max.	3,4	3,3	3,6	ns	

For **switching times waveforms** see Family Specifications.

QUINT D-LATCH

The 10175 includes five D-latches with common reset and two wired-OR common clock inputs. When the clock is in the HIGH state, any change of the data input does not affect the output state. When the clock is in the LOW state, any change of the data input is transferred at the output. The outputs are latched on the positive transition of the clock. The reset input is enabled only when the clock is HIGH. All unused inputs must be tied LOW to V_{IL} or V_{EE}.

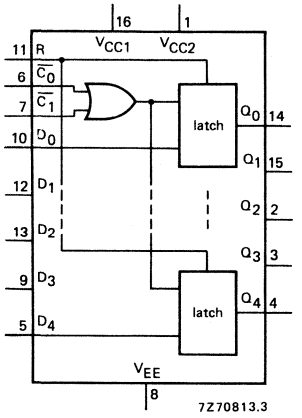


Fig. 1 Logic diagram.

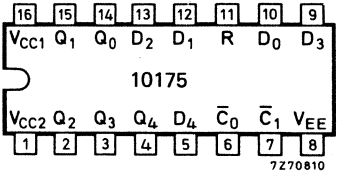


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	400 mW

PACKAGE OUTLINES (see Package Outlines)

10175N: plastic 16-lead dual in-line (SOT-38).
10175F: ceramic 16-lead dual in-line (SOT-74).

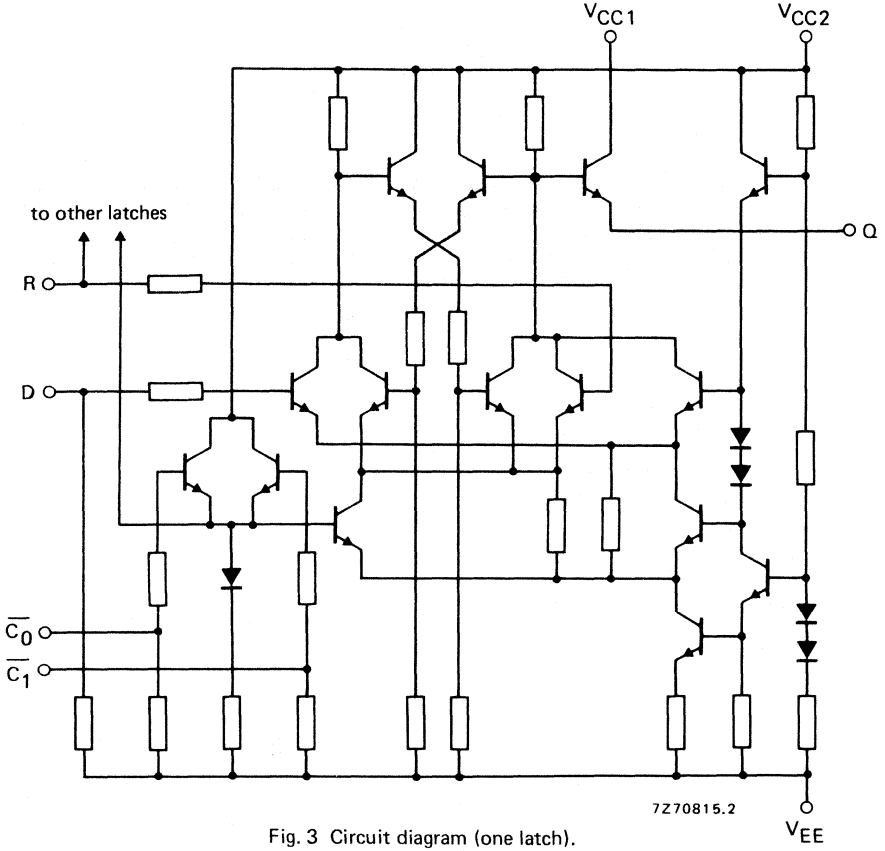


Fig. 3 Circuit diagram (one latch).

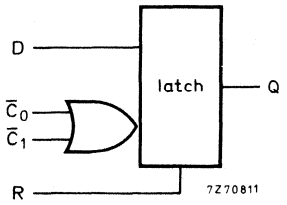


Fig. 4 Logic function.

FUNCTION TABLE

$\overline{C}_0$	$\overline{C}_1$	R	D	Q_{n+1}
L	L	X	L	L
L	L	X	H	H
H	X	L	X	Q_n
X	H	L	X	Q_n
H	X	H	X	L
X	H	H	X	L

Positive logic:
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

FAMILY DATA and **RATINGS** see Family Specifications

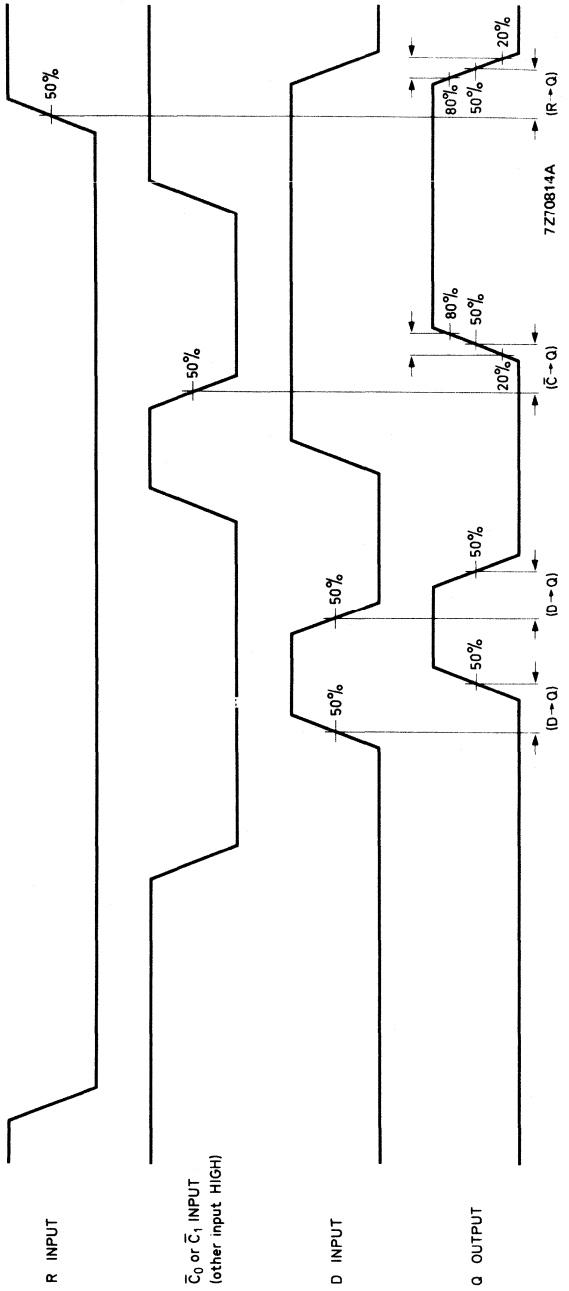


Fig. 5 Switching times waveforms.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	107	97	107	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	11	1000	650	650	μA	
		5,6,7,9,	460	290	290	μA	
		10,12,13	460	290	290	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For Q_n, D_n at V_{IHmax} Other inputs at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	All inputs at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For Q_n, D_n at V_{IHC} Other inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For Q_n, D_n at V_{ILC} Other inputs at V_{ILmin}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise and fall propagation delay times	$\frac{t_{PLH}}{t_{PHL}}$						
D → Q		min.	1,0	1,0	1,0	ns	Data to output
		max.	3,6	3,5	3,6	ns	
C → Q		min.	1,0	1,0	1,0	ns	Clock to output
		max.	4,7	4,3	4,4	ns	
R → Q		min.	1,0	1,0	1,0	ns	Reset to output
		max.	4,0	3,9	4,2	ns	
Rise and fall transition time	$\frac{t_{TLH}}{t_{THL}}$	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,6	3,5	3,7	ns	
Set-up time	T_s	min.	2,5	2,5	2,5	ns	
Hold time	T_h	min.	1,5	1,5	1,5	ns	

Notes: Propagation delay from reset to output. Output latched on a HIGH state prior to test.

Set-up times are the minimum times before the positive transition of the clock pulse (C) that information must be held at the data inputs (D).

Hold times are the minimum times after the positive transition of the clock pulse (C) that information must be held at the data inputs (D).

For **switching times test circuit** and **waveforms** see Family Specifications.

HEX D-TYPE MASTER-SLAVE FLIP-FLOP

The 10176 includes six high speed master-slave D-type flip-flops with one common input clock for all six. Data enters into the master during the LOW state of the clock and is transferred to the slave during the positive-going clock transition. Due to the master-slave structure of the device, a change in the information present at the data (D) input will not modify the output information at any other time. All unused inputs must be tied LOW to V_{IL} or V_{EE}.

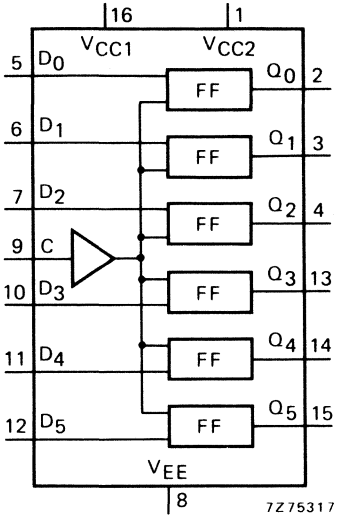


Fig. 1 Logic diagram.

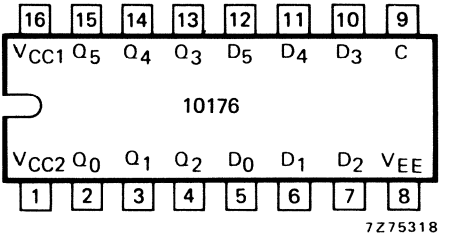


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Clock frequency	fc	typ. 150	MHz
Output voltage			
HIGH state	V_{OH}	nom. −880	mV
LOW state	V_{OL}	nom. −1720	mV
Power consumption per package (no load)	P_D	typ. 460	mW

PACKAGE OUTLINES (see Package Outlines)

10176N: plastic 16-lead dual in-line (SOT-38).
10176F: ceramic 16-lead dual in-line (SOT-74).

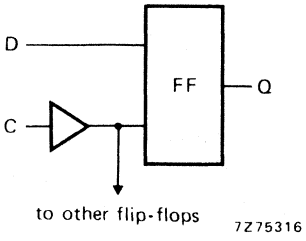


Fig. 3 Logic diagram (one flip-flop).

FUNCTION TABLE

C	D	$Q_n + 1$
L	X	Q_n
H	L	L
H	H	H

Positive logic: HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

C at LOW state; data enters into the master. A clock H means a clock transition from a LOW to a HIGH state; data transfer to the slave output.

RATINGS and **FAMILY DATA** see Family Specifications.

D.C. CHARACTERISTICS

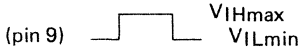
V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	121	110	121	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	9	495	310	310	μA	
		other pins	350	220	220	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	All inputs at V_{IHmax} (Note 1)
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	All inputs at V_{ILmin} (Note 1)
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC} (Note 1)
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC} (Note 1)

Note 1: Output level to be measured after a clock pulse has been applied



A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,6	1,6	1,6	ns	50% to 50%
		max.	4,6	4,5	5,0	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,1	1,1	ns	20% to 80%
		max.	4,1	4,0	4,4	ns	
Set-up time D → C	t_{DSC}	min.	2,5	2,5	2,5	ns	
Hold time C → D	t_{CHD}	min.	1,5	1,5	1,5	ns	
Clock frequency	f_c	min.	125	125	125	MHz	

For **switching times test circuit** and **waveforms** see Family Specifications.

LOOK-AHEAD CARRY BLOCK

The 10179 is a look-ahead carry block. It can be used in conjunction with the 10181 4-bit arithmetic/logic unit to perform a high order look-ahead carry, in applications requiring high speed arithmetic operation on long words.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

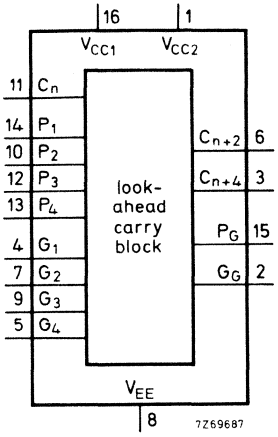


Fig. 1 Block diagram.

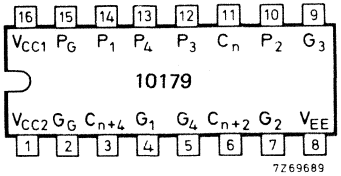


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5,2$ V.

C_n:	carry input
P_2 to P_4:	carry propagate inputs
G_1 to G_4:	carry generate inputs
$C_n + 2$; $C_n + 4$:	carry outputs
P_G:	carry propagate output*
G_G:	carry generate output*

* For higher order look-ahead extension.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	300 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10179N: plastic 16-lead dual in-line (SOT-38).
10179F: ceramic 16-lead dual in-line (SOT-74).

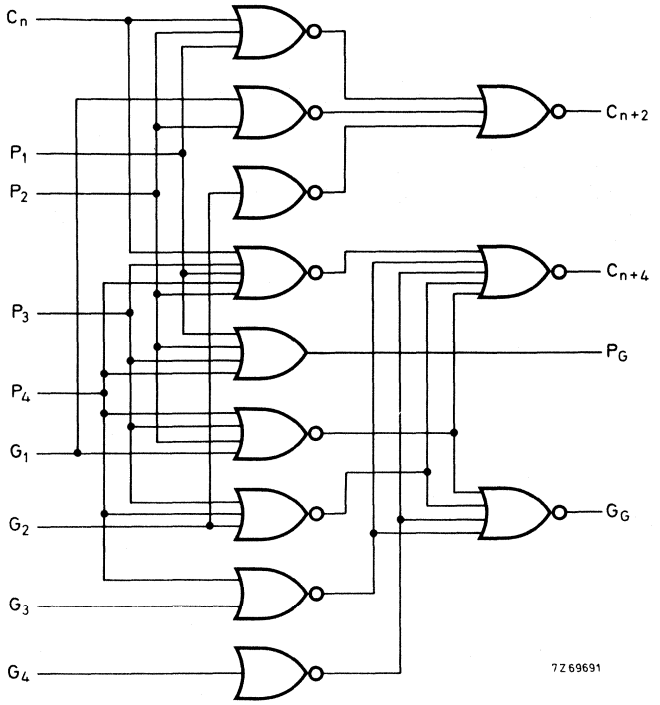


Fig. 3 Logic diagram.

LOGIC FUNCTION

$P_G = P_1 + P_2 + P_3 + P_4$

$G_G = G_4 (G_3 + P_4) (G_2 + P_3 + P_4) (G_1 + P_2 + P_3 + P_4)$

$C_{n+2} = G_2 (G_1 + P_2) (C_n + P_1 + P_2)$

$C_{n+4} = G_4 (G_3 + P_4) (G_2 + G_3 + P_4) (G_1 + P_2 + P_3 + P_4) (C_n + P_1 + P_2 + P_3 + P_4)$

In positive logic: H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

The overall carry function is invariant with the polarity (positive or negative) of the logic if the P and G inputs are interchanged.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	79	72	79	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	5,9	360	225	225	μA	
		4,7,11	430	270	270	μA	
		14	565	355	355	μA	
		12	630	395	395	μA	
		10,13	700	440	440	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	For output 2 pins 4, 5, 7, 9 at V_{IHmax}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	For output 2 pins 4, 7, 7, 9 at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	For output 2 pin 13 at V_{IHmax} pin 5 at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	For output 2 pin 13 at V_{IHmax} pin 5 at V_{ILC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
$P \rightarrow P_g$	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		max.	3,7	3,5	3,9	ns	
$C_n \rightarrow C$		min.	1,0	1,0	1,0	ns	
		max.	5,8	4,5	6,1	ns	
$G \rightarrow C$		min.	1,0	1,0	1,0	ns	
$G \rightarrow G_g$		max.	5,8	5,5	6,1	ns	
$P \rightarrow G_g$							
Transition rise and fall time	t_{THL}/ t_{TLH}	min.	1,1	1,1	1,1	ns	between 20% and 80%
		typ.		2,5			
		max.	3,7	3,5	3,9	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 2-BIT ADDER/SUBTRACTOR

The 10180 is a high-speed, low power, general purpose adder/subtractor. Inputs for each adder are: Carry-in, Operand A, Operand B. Outputs are: Sum, $\overline{\text{Sum}}$ and Carry-out.
Common select inputs act as control lines to invert A or B for subtract. A very high speed of operation is possible with Operand in the Sum or Carry-out propagation delay of 4,5 ns, and Carry-in to Carry-out propagation delay of 2,2 ns.
The 10180 is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays.
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

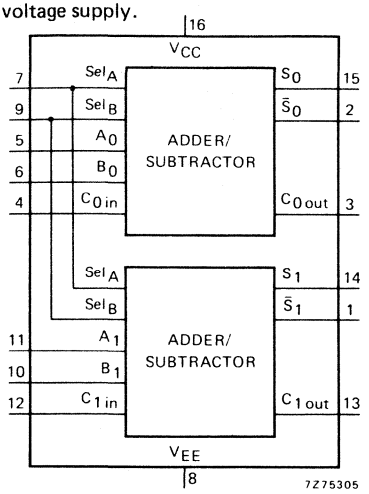


Fig. 1 Block diagram.

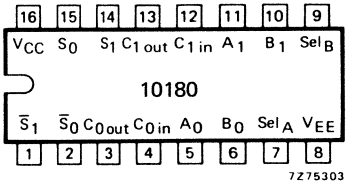


Fig. 2 Pin designation.

V_{CC} = 0 V (ground)
V_{EE} = -5,2 V

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay Address to C_{OUT}	t_{PLH}	typ.	4,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	360 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10180N: plastic 16-lead dual in-line (SOT-38).
10180F: ceramic 16-lead dual in-line (SOT-74).

FUNCTION SELECT TABLE

Sel_A	Sel_B	functions S
H	H	$A + B + C_I$
H	L	$C_I + A - B$
L	H	$C_I + B - A$
L	L	$C_I - A - B$

Positive logic: HIGH state = 1
(the more positive voltage)
LOW state = 0
(the less positive voltage)

Positive logic only

$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

Both positive and negative logic

$S = \overline{C}_{in}\,(\overline{A}'\,B' + A'\,\overline{B}') + C_{in}\,(A'\,B' + \overline{A}'\,\overline{B}')$

$C_{out} = C_{in}\,A' + C_{in}\,B' + A'\,B'$

FUNCTION TABLE

function	inputs					outputs		
	Sel_A	Sel_B	A	B	C_{in}	S	$\overline{S}$	C_{out}
ADD ($A + B + C_I$)	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT ($C_I + A - B$)	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
Reverse SUBTRACT ($C_I + B - A$)	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
($C_I - A - B$)	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

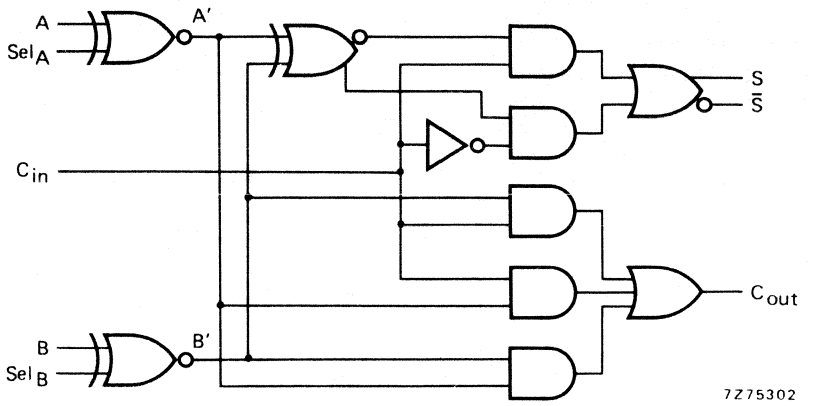


Fig. 3 Logic function (one adder/subtractor).

RATINGS see Family Specifications

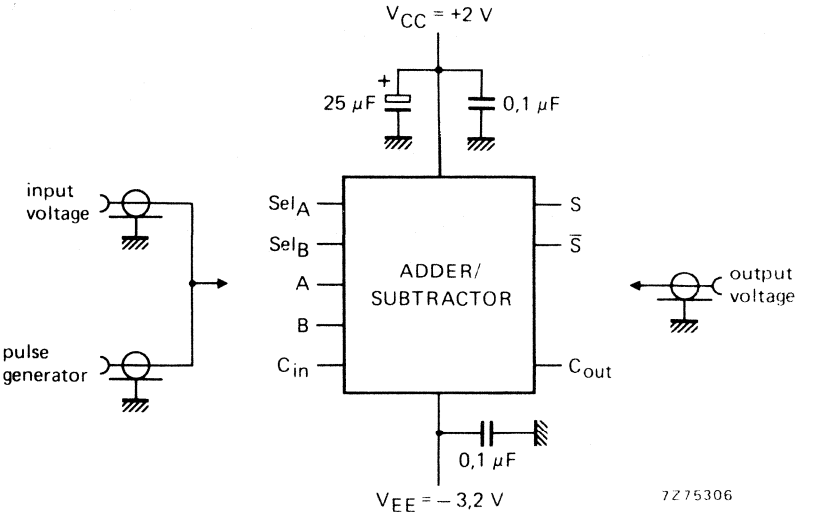


Fig. 4 Switching times test circuit.
Input pulse condition: $t_r = t_f = 2{,}0 \pm 0{,}2$ ns (20 to 80%)

For **switching times waveforms** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	95	86	95	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test section"
Input current HIGH	I_{IHmax}	5,6,10,11	350	220	220	μA	
		7,9	460	290	290	μA	
		4,12	590	370	370	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	All input/output combination in accordance with the function table. Input conditions: V_{ILmin} or V_{IHmax} for V_{OH} and V_{OL}. V_{ILC} or V_{IHC} for V_{OHC} and V_{OLC}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay rise and fall times	t_{PLH} t_{PHL}						
A → C_{out}		min.	1,3	1,3	1,1	ns	Operand to output
SEL → C_{out}		max.	5,8	5,4	5,8	ns	Select to output
C_i → C_{out}		min.	1,0	1,0	0,9	ns	Carry in to out
		max.	3,4	3,3	3,6	ns	
Transition rise and fall times	t_{TLH} t_{THL}	min.	1,0	1,1	1,1	ns	between 20% and 80%
		max.	3,8	3,7	3,9	ns	

For **switching times waveforms** see Family Specifications.

4-BIT ARITHMETIC/LOGIC UNIT

The 10181 is a high-speed arithmetic logic unit. It performs 16 logic operations and 16 arithmetic operations on two 4-bit words. Arithmetic or logic mode of operation is selected by the mode control input (M). Arithmetic logic operations are selected by a 4-bit select input (S_0 to S_3) in accordance with the function table. The device provides a group carry propagate (P_G) and a carry generate (G_G) for high-speed operations on very long words, using a 10179 as a high order look-ahead carry block. The internal carry is enabled while the mode control input (M) is LOW (arithmetic operation).
Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

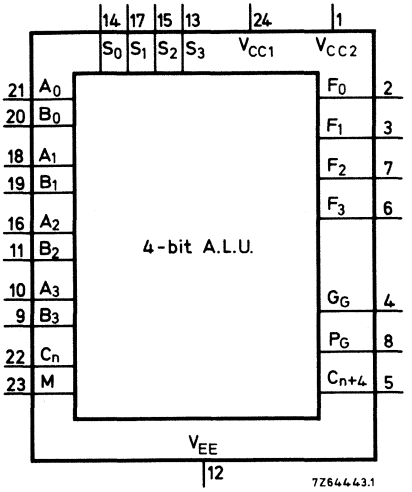


Fig. 1 Block diagram.

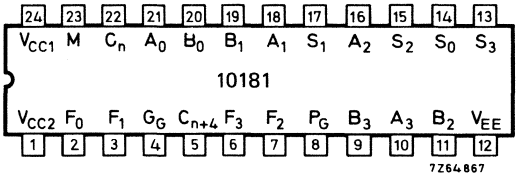


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PLH}	typ.	4,2 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	600 mW

PACKAGE OUTLINES (see Package Outlines)

10181N: plastic 24-lead dual in-line (SOT-101).
10181F: ceramic 24-lead dual in-line (SOT-149).

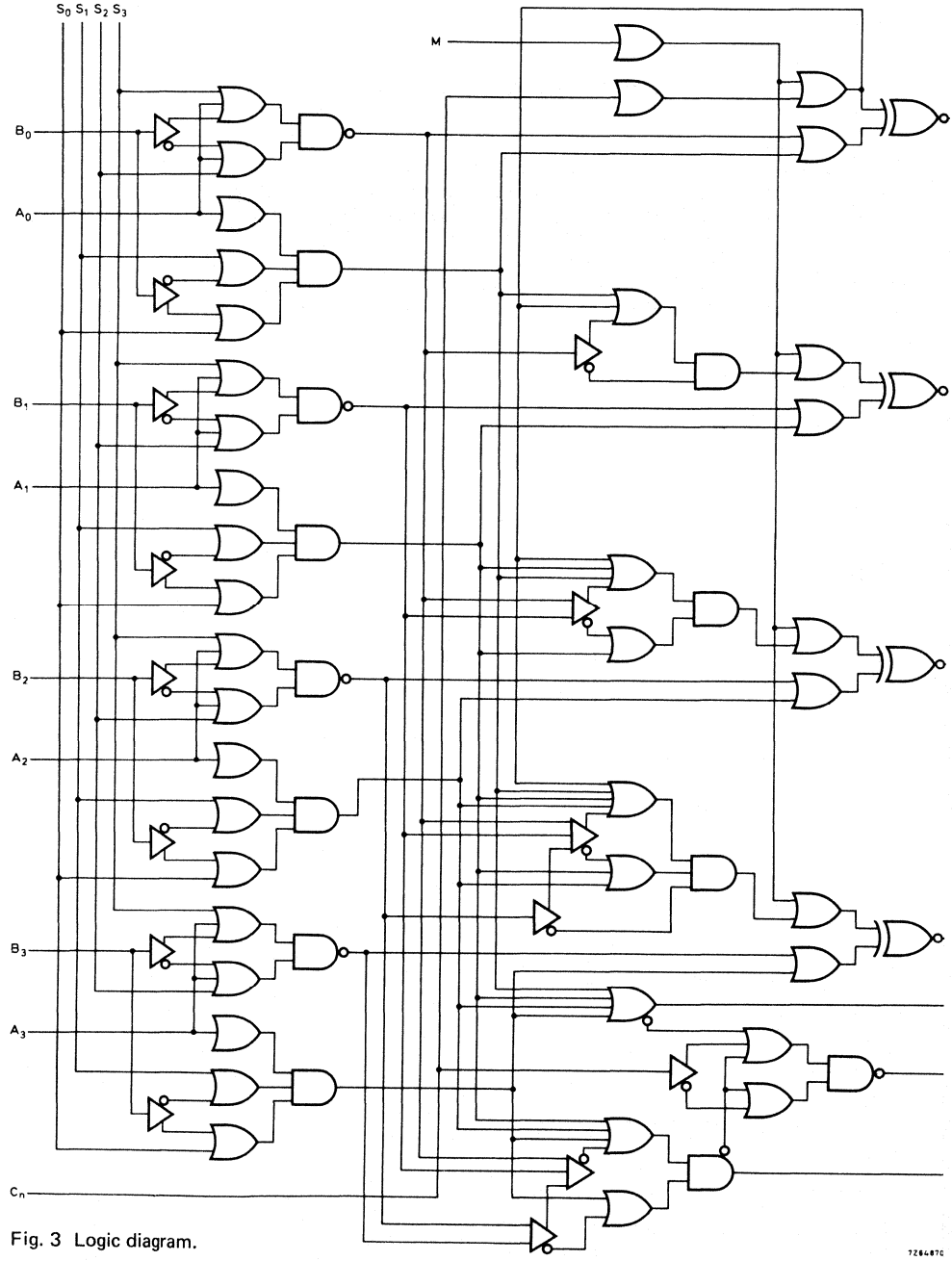


Fig. 3 Logic diagram.

PIN NAMES

A_0 to A_3: word inputs
B_0 to B_3: word inputs
S_0 to S_3: function select inputs
M : mode control input
F_0 to F_3: data outputs

C_n : carry input
C_{n+4}: carry output
P_G : carry propagate output
G_G : carry generate output

FUNCTION TABLE

function select inputs				logic function mode	arithmetic operation mode
S_3	S_2	S_1	S_0	F (M = HIGH)	F (M = LOW; C_n = LOW)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A} + \overline{B}$	A plus ($A \cdot \overline{B}$)
L	L	H	L	$\overline{A} + B$	A plus ($A \cdot B$)
L	L	H	H	logic "1"	A times 2
L	H	L	L	$\overline{A \cdot B}$	(A+B) plus 0
L	H	L	H	$\overline{B}$	(A+B) plus ($A \cdot \overline{B}$)
L	H	H	L	$AB + A\overline{B}$	A plus B
L	H	H	H	$A + \overline{B}$	A plus (A+B)
H	L	L	L	$\overline{A} \cdot B$	($A+\overline{B}$) plus 0
H	L	L	H	$A\overline{B} + \overline{A}B$	A minus B minus 1
H	L	H	L	B	($A+\overline{B}$) plus ($A \cdot B$)
H	L	H	H	A + B	A plus ($A+\overline{B}$)
H	H	L	L	logic "0"	minus 1 (two's complement)
H	H	L	H	$A \cdot \overline{B}$	($A \cdot \overline{B}$) minus 1
H	H	H	L	AB	($A \cdot B$) minus 1
H	H	H	H	A	A minus 1

Positive logic: H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS and **FAMILY DATA** see Family Specifications.

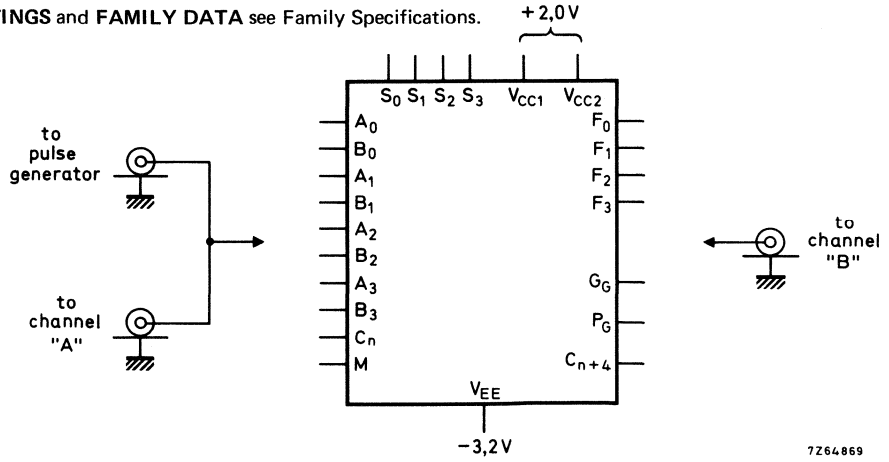


Fig. 4 Switching times test circuit.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	12	159	145	159	mA	
Input current LOW	I_{ILmin}	9	0.5	0.5	0.3	μA	
Input current HIGH	I_{IHmax}	9,11,19,20	390	245	245	μA	see "How to test Section"
		10,16,18,21	350	220	220	μA	
		23	320	200	200	μA	
		13,14,15,17	425	265	265	μA	
		22	460	290	290	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	All input/output combination in accordance with the function table. Input condition: V_{IHmax} or V_{ILmin} for V_{OH} and V_{OL}, V_{IHC} or V_{ILC} for V_{OHC} and V_{OLC}
		typ.		− 860		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	

See also Family Specifications **switching times test circuit and waveforms.**

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	T_{amb} (°C)						unit	remark
		−30		+25		+85			
propagation delay rise and fall times	$\frac{t_{PLH}}{t_{PHL}}$	min.	max.	min.	max.	min.	max		
$C_n \rightarrow C_{n+4}$		1,0	5,1	1,1	5,0	1,1	5,4	ns	
$C_n \rightarrow F$		1,7	7,2	2,0	7,0	2,0	7,5	ns	
$A \rightarrow F$		2,6	10,4	3,0	10,0	3,0	10,8	ns	
$A \rightarrow P_g$		1,6	7,0	2,0	6,5	2,0	7,0	ns	
$A \rightarrow G_g$		1,1	7,4	2,0	7,0	1,3	7,7	ns	
$A \rightarrow C_{n+4}$		1,7	7,3	2,0	7,0	2,0	7,8	ns	
$B \rightarrow F$		2,7	11,3	3,0	11,0	3,0	11,9	ns	
$B \rightarrow P_g$		1,6	7,7	2,0	7,5	2,0	8,0	ns	
$B \rightarrow G_g$		1,7	8,2	2,0	8,0	2,0	8,6	ns	
$B \rightarrow C_{n+4}$		1,8	8,2	2,0	8,0	2,0	8,7	ns	
$M \rightarrow F$		2,4	10,3	3,0	10,0	3,0	10,8	ns	
$S \rightarrow F$		2,5	10,7	3,0	10,0	3,0	10,8	ns	
$S \rightarrow P_g$		1,7	8,3	2,0	8,0	2,0	8,4	ns	
$S \rightarrow G_g$		1,5	9,6	2,0	9,0	1,9	9,7	ns	
$S \rightarrow C_{n+4}$		1,6	9,3	2,0	9,0	2,0	9,9	ns	
Transition rise and fall times	$\frac{t_{TLH}}{t_{THL}}$								
Output C_{n+4}	C_n	1,0	3,2	1,0	3,0	1,0	3,2	ns	
	A	1,0	3,1	1,0	3,0	1,0	3,2	ns	
	B	0,9	3,1	1,0	3,0	1,0	3,2	ns	
	S	0,9	5,3	1,1	5,0	1,0	5,2	ns	
Output F	C_n	1,3	5,3	1,5	5,0	1,5	5,3	ns	
	A	1,3	5,4	1,5	5,0	1,5	5,3	ns	
	B	1,2	5,3	1,5	5,0	1,5	5,3	ns	
	M	1,1	5,1	1,5	5,0	1,5	5,3	ns	
	S	1,0	5,4	1,5	5,0	1,5	5,4	ns	
Output P_g	A	0,8	3,7	1,1	3,5	1,1	3,8	ns	
	B	1,0	3,6	1,1	3,5	1,1	3,9	ns	
	S	0,8	5,1	1,1	5,0	1,1	5,2	ns	
Output G_g	A	1,2	5,1	1,5	5,0	1,2	5,3	ns	
	B	1,4	5,2	1,5	5,0	1,2	5,4	ns	
	S	0,8	6,2	0,8	6,0	0,8	6,5	ns	

HEX BUFFER WITH ENABLE

The 10188 includes six buffers offering individual inputs and outputs and a common enable input, driving all outputs LOW. Each input is connected to V_{EE} via a pull-down resistor resulting in high input impedance and eliminating need of connecting unused inputs LOW.

Due to open emitter outputs the 10188 features OR capability with high fan-out for driving 50 Ω lines.

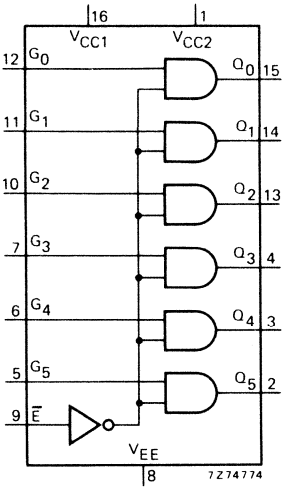


Fig. 1 Logic diagram.

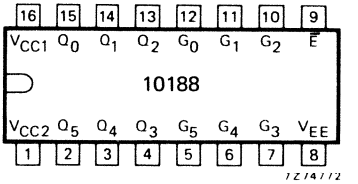


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}	−30 to	+85 °C
Average propagation delay	t_{PLH}	typ.	2,0 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	170 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (See Package Outlines)

10188N: plastic 16-lead dual in-line (SOT-38).
10188F: ceramic 16-lead dual in-line (SOT-74).

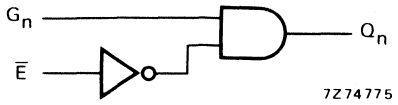


Fig. 3 Logic diagram (one buffer).

FUNCTION TABLE

inputs		output
$\overline{E}$	G_n	Q_n
L	L	L
L	H	H
H	X	L

LOGIC FUNCTION

$Q_n = G_n . \overline{E}$

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

RATINGS see Family Specifications

For **switching times test circuit** and **waveform** see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	46	42	46	mA	
Input current	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current	I_{IHmax}	9	460	290	290	μA	
		other inputs	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	$\overline{E}$ at V_{ILmin}
		typ.		− 880		mV	Other inputs at
		max.	− 890	− 810	− 700	mV	V_{IHmax}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	V	All inputs at at V_{ILmin}
		typ.		−1 720		V	
		max.	−1 675	−1 650	−1 615	V	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC} Other inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	V	One input at V_{ILC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
$G_n \rightarrow Q_n$	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	Data to output
		max.	3,3	2,9	3,3	ns	
$\overline{E} \rightarrow Q_n$		min.	1,1	1,1	0,1	ns	Enable to output
		max.	3,9	3,5	3,9	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0			20% to 80%
		max.	3,7	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

HEX INVERTER WITH ENABLE

The 10189 includes six inverters offering individual inputs and outputs and a common enable input, driving all outputs LOW. Each input is connected to V_{EE} via a pull-down resistor resulting in high input impedance and eliminating the need of tying unused inputs LOW. Due to open emitter outputs the 10189 features OR capability with high fan-out for driving 50 Ω lines.

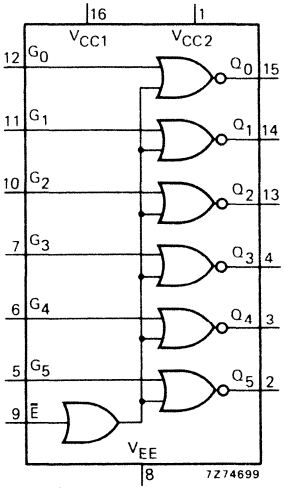


Fig. 1 Logic diagram.

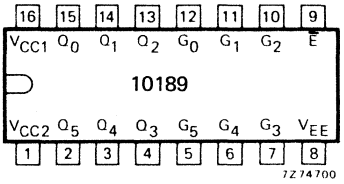


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PLH}	typ.	2 ns
Output voltage HIGH state	V_{OH}	nom.	−880 mV
Output voltage LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	180 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10189N: plastic 16-lead dual in-line (SOT-38).
10189F: ceramic 16-lead dual in-line (SOT-74).

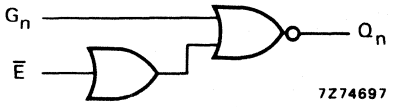


Fig. 3 Logic diagram (one inverter).

LOGIC FUNCTION

$Q_n = \overline{G_n + E}$

Positive logic

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	44	40	44	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current	I_{IHmax}	9	890	555	555	μA	
		other pins	425	265	265	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	All inputs at V_{ILmin}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	$\overline{E}$ at V_{IHmax} Other inputs at V_{ILmin}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{ILC} Other inputs at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
$G_n \rightarrow Q_n$	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,0		ns	Data to output
		max.	3,3	2,9	3,3	ns	
$\bar{E} \rightarrow Q_n$		min.	1,1	1,1	0,1	ns	Enable to output
		max.	3,9	3,5	3,9	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	
		typ.		2,0			20% to 80%
		max.	3,6	3,3	3,7	ns	

For **switching times test circuit** and **waveform** see Family Specifications.

HEX ECL-MST TRANSLATOR

It includes six gates offering individual inputs and outputs and a common enable input, driving all outputs LOW when in the HIGH state. Each input is connected to V_{EE} via a pull-down resistor emitter outputs the 10191 features OR capability with high fan-out for driving 50 Ω lines.

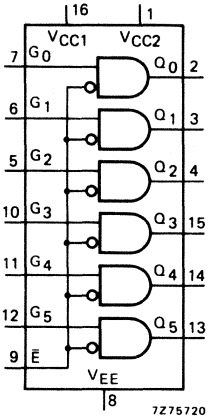


Fig. 1 Circuit diagram.

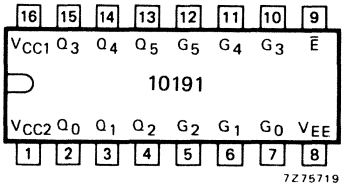


Fig. 2 Pinning diagram.

V_{CC2} = +1,25 V
V_{EE} = −5,2 V.
V_{CC1} = 0 V (ground)

QUICK REFERENCE DATA

Supply voltage	V_{EE}	−5,2 ± 10%	V
Operating ambient temperature range	T_{amb}	−30 to +85	°C
Average propagation delay	t_{PLH}	typ. 2,2	ns
Power consumption per package (no load)	P_D	typ. 180	mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10191N: plastic 16-lead dual in-line (SOT-38).
10191F: ceramic 16-lead dual in-line (SOT-74).

Fig. 3 Logic diagram (one gate).

LOGIC FUNCTION

$Q_n = G_n . \overline{E}$

FUNCTION TABLE

inputs		output
$\overline{E}$	G_n	Q_n
L	L	L
L	H	H
H	X	L

Positive logic
H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0
X = state is immaterial

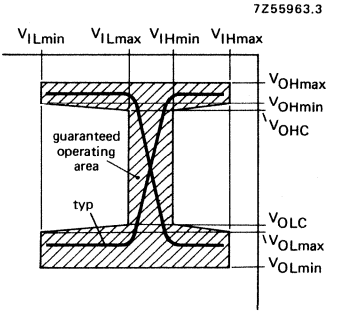


Fig. 4 Transfer characteristics.

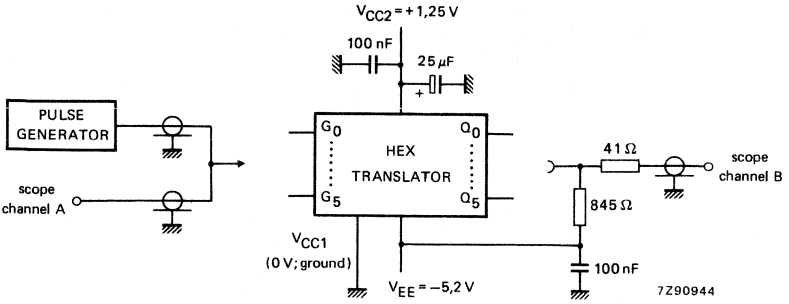


Fig. 5 Switching time test circuit.
Input pulse condition $t_{TLH} = t_{THL} = 2{,}0 \pm 0{,}2$ ns (20 to 80%).

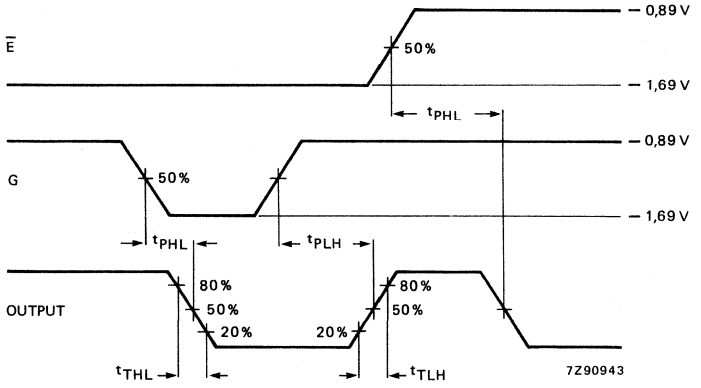


Fig. 6 Switching times waveforms.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V; V_{CC2} = +1.25 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	39	35	39	mA	
	I_{CCmax}	1	23	23	23	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current	I_{IHmax}	9	425	265	265	μA	
		other pins	390	245	245	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	374	440	548	mV	For output: 2 pin 7 at V_{IHmax} and pin 9 at V_{ILmin}
		max.	156	255	327	mV	
Output voltage LOW	V_{OL}	min.	−523	−490	−454	mV	For each output Pin 9 at V_{ILmin}
		max.	−323	−290	−254	mV	
Output threshold voltage HIGH	V_{OHC}	min.	136	235	307	mV	For output 2: pin 7 at V_{IHC} and pin 9 at V_{ILmin}
Output threshold voltage LOW	V_{OLC}	max.	−303	−270	−234	mV	For output 2: pin 7 at V_{ILC} and pin 9 at V_{ILmin}

A.C. CHARACTERISTICS

V_{CC1} = ground; V_{EE} = −5.2 V; V_{CC2} = 1.25 V

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times							
$G_n \rightarrow Q_n$	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	
		typ.		2,2		ns	Data to output
		max.	3,6	3,4	3,7	ns	
$\overline{E} \rightarrow Q_n$		min.	1,0	1,0	1,0	ns	
		max.	4,7	4,5	5,0	ns	Enable to output
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,1	1,1	1,1	ns	20% to 80%
		typ.	4.5	4,3	4,7	ns	

For switching times test circuit and waveforms see Fig. 5 and 6.

QUADRUPLE CURRENT-MODE BUS DRIVER

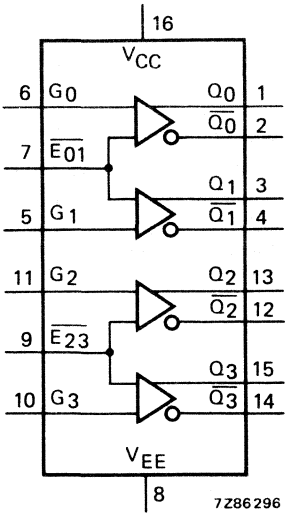


Fig. 1 Logic diagram.

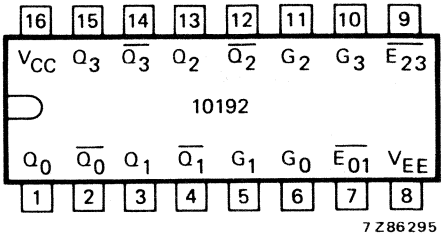


Fig. 2 Pin designation.
V_{CC} = 0 V (ground); V_{EE} = −5,2 V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{PHL}/t_{PLH}	typ.	4,0 ns
Power consumption per package (no load)	P_D	typ.	490 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see Package Outlines)

10192N: plastic 16-lead dual in-line (SOT-38).
10192F: ceramic 16-lead dual in-line (SOT-74).

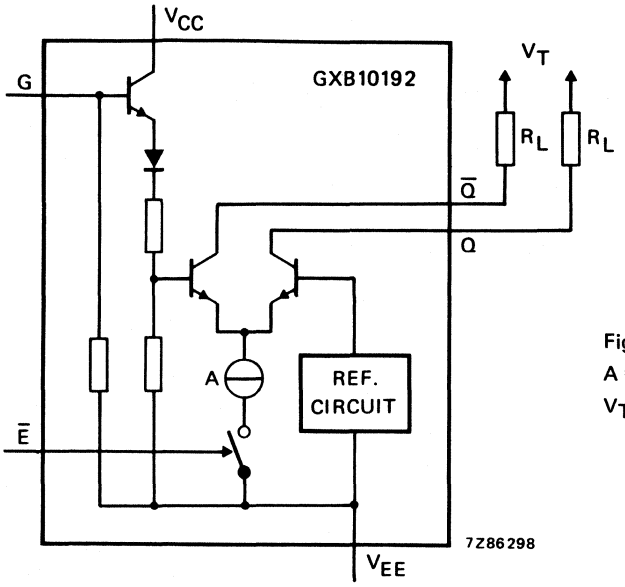


Fig. 3 Simplified circuit diagram.

A = 16 mA switched current source.

V_T should not exceed + 5,5 V and R_L and V_T should be chosen so that V_Q does not go more negative than −2,4 V

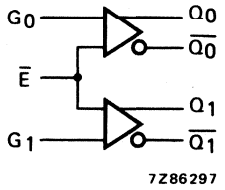


Fig. 4 Logic function.

Function table

inputs		output			
		current		voltage	
$\overline{E}$	G	$\overline{Q}$	Q	$\overline{Q}$	Q
L	L	L	H	H	L
L	H	H	L	L	H
H	X	L	L	H	H

Positive logic HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

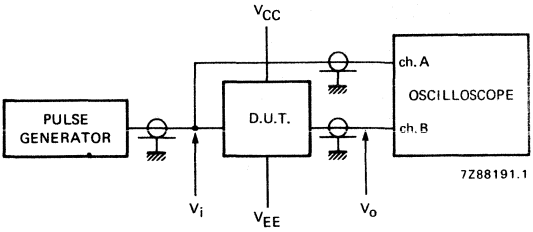
X = state is immaterial

Basic driver operation.

$V_{OH} = V_T$

$V_{OL} = V_T - 0{,}016.\ R_L$ (typ.)

FAMILY DATA and **RATINGS** see Family Specifications.



input pulse
$t_r = t_f = 2{,}0 \pm 0{,}2$ ns (20 to 80%)

Fig. 5 Switching times test circuit.

$V_{CC} = 0$ V (ground); $V_{EE} = -5{,}2$ V.

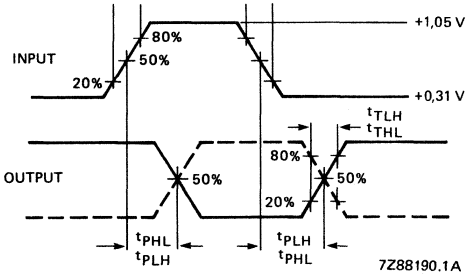


Fig. 6 Switching times waveforms.

Notes

1. Non-specified input pins should be connected to V_{ILmin} or left open.
2. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
3. Input impedance of the oscilloscope is 50 Ω.
4. The unmatched wire stub between coaxial cable and pins under test must be less than 6 mm long for proper tests.

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground; $V_{EE} = -5{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Input current HIGH	I_{IH}	max.	510	320	330	μA	
Input current LOW	I_{IL}	min.	0,5	0,5	0,3	μA	
Supply current	I_{EE}	max.	72	65	72	mA	
Output current HIGH	I_{OH}	min.	13,5	14,0	14,0	mA	For non-inverted output $V_I = V_{IHmax}$; $R_L = 50\ \Omega$ to ground For inverted output $V_I = V_{ILmin}$; $R_L = 50\ \Omega$
		max.	18,0	18,0	18,5	mA	
LOW	I_{OL}	max.	1,0	1,0	1,0	mA	Reverse conditions at input level
Output voltage LOW	V_{OL}	min.	−2,4	−2,4	−2,4	V	For non-inverted output $V_I = V_{ILmax}$ For inverted output $V_I = V_{IHmax}$ $R_L = 50\ \Omega$ to ground

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -3{,}2$ V

	symbol		T_{amb} (°C) −30	T_{amb} (°C) +25	T_{amb} (°C) +85	unit	remarks
Rise and fall propagation delay times	t_{PLH} / t_{PHL}						
D → Q		min.	1,5	1,5	1,5	ns	
		max.	4,8	4,8	5,1	ns	
$\overline{E}$ → Q		min.	2,0	2,0	2,0	ns	
		max.	6,3	6,0	6,6	ns	
Transition rise and fall times	t_{TLH}	min.	1,3	1,3	1,3	ns	between 20% and 80%
	t_{THL}	max.	3,5	3,3	3,7	ns	

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT OR LINE DRIVER

The 10210 is a high speed dual 3-input/3-output OR gate intended to drive up to six transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications. The 10210 is a higher speed version of the 10110. It is a pin-for-pin replacement for the device. Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

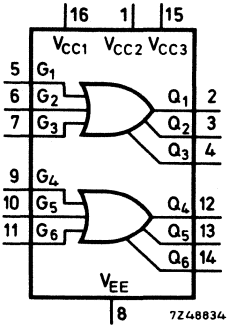


Fig. 1 Logic diagram.

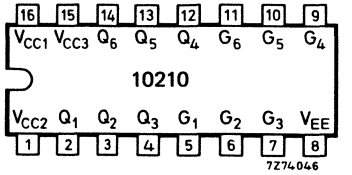


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Average propagation delay	t_{PHL}	typ.	1,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	160 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10210N: plastic 16-lead dual in-line (SOT-38).
10210F: ceramic 16-lead dual in-line (SOT-74).

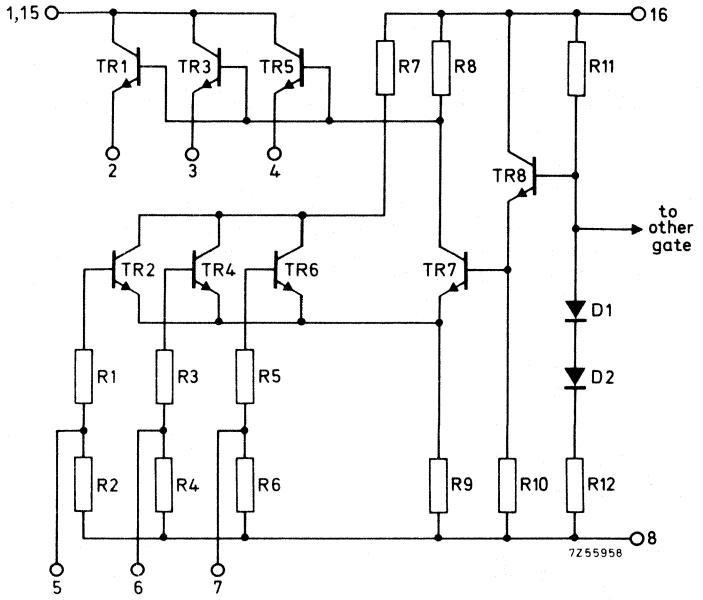


Fig. 3 Circuit diagram (one gate).

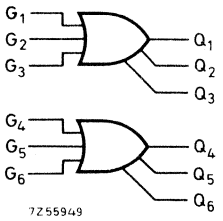


Fig. 4 Logic function.

$Q_1 = Q_2 = Q_3 = G_1 + G_2 + G_3$

$Q_4 = Q_5 = Q_6 = G_4 + G_5 + G_6$

Positive logic: HIGH state = 1
LOW state = 0

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	42	38	42	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	5*	650	410	410	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	One input
		typ.		− 880		mV	at
		max.	− 890	− 810	− 700	mV	V_{IHmax}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	Inputs
		typ.		−1 720		mV	at
		max.	−1 675	−1 650	−1 615	mV	V_{ILmin}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{ILC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	All outputs
		typ.		1,5		ns	loaded
		max.	2,6	2,5	2,8	ns	50% to 50%
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,0	1,0	ns	All outputs
		typ.		1,3		ns	loaded
		max.	2,6	2,5	2,6	ns	20% to 80%

For **switching times test circuit** and **waveforms** see Family Specifications.

DUAL 3-INPUT/3-OUTPUT NOR LINE DRIVER

The 10211 is a high speed dual 3-input/3-output NOR gate intended to drive up to three transmission lines simultaneously. This feature makes the device particularly useful in clock distribution applications.

The 10211 is a higher speed version of the 10111. It is a pin-for-pin replacement for this type. Unused inputs can be left open due to integrated pull-down resistors, which avoids the need for a voltage supply.

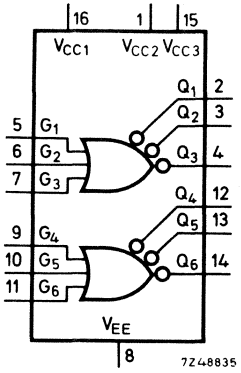


Fig. 1 Logic diagram.

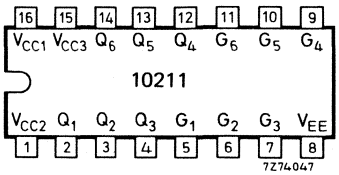


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = V_{CC3} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay	t_{pd}	typ.	1,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	160 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10211N: plastic 16-lead dual in-line (SOT-38).
10211F: ceramic 16-lead dual in-line (SOT-74).

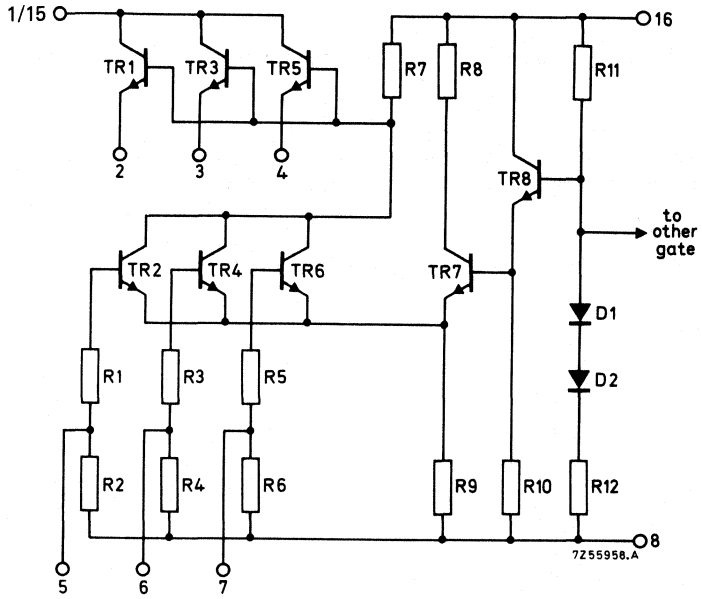
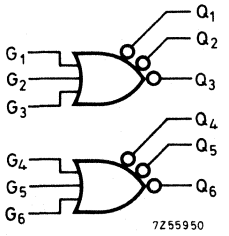


Fig. 3 Circuit diagram.



$Q_1 = Q_2 = Q_3 = \overline{G_1 + G_2 + G_3}$

$Q_4 = Q_5 = Q_6 = \overline{G_4 + G_5 + G_6}$

Positive logic: HIGH state = 1
LOW state = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	42	38	42	mA	
Input current LOW	I_{ILmin}	5*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	5*	650	410	410	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	Inputs
		typ.		− 880		mV	at
		max.	− 890	− 810	− 700	mV	V_{ILmin}
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	One input
		typ.		−1 720		mV	at
		max.	−1 675	−1 650	−1 615	mV	V_{IHmax}
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	One input at V_{ILC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	One input at V_{IHC}

A.C. CHARACTERISTICS

V_{CC1} = V_{CC2} = 2.0 V; V_{EE} = −3.2 V; R_L = 50 Ω to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	All outputs
		typ.		1,5		ns	loaded
		max.	2,6	2,5	2,8	ns	50% to 50%
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,0	1,0	ns	All outputs
		typ.		1,3		ns	loaded
		max.	2,6	2,5	2,8	ns	20% to 80%

For **switching times test circuit** and **waveforms** see Family Specifications.

HIGH SPEED TRIPLE LINE RECEIVER

The 10216 is a high speed, triple differential amplifier designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger or in other applications where a stable reference voltage is necessary. Active current sources provide the 10216 with excellent common mode noise rejection. If any amplifier in a package is not used the input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

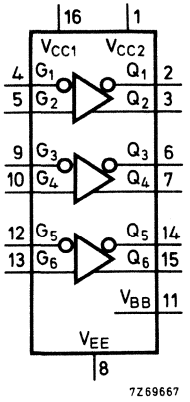


Fig. 1 Logic diagram.

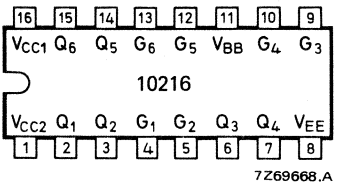


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = 5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Average propagation delay			
single-ended input	t_{PLH}	typ.	1,8 ns
differential input	t_{PLH}	typ.	1,5 ns
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	100 mW

FAMILY DATA see Family Specifications.

PACKAGE OUTLINES (see Package Outlines)

10216N: plastic 16-lead dual in-line (SOT-38).
10216F: ceramic 16-lead dual in-line (SOT-74).

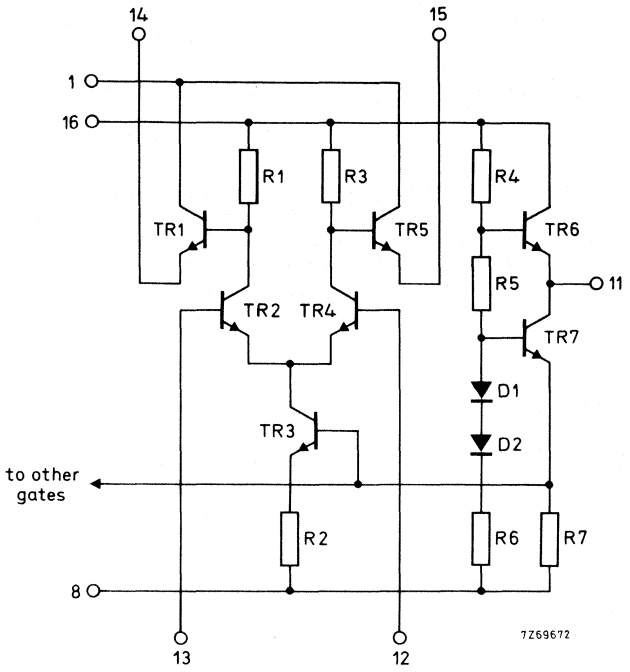
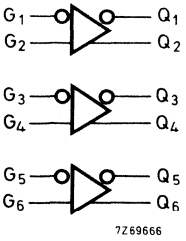


Fig. 3 Circuit diagram (one amplifier).



With inputs G_2, G_4 and G_6 connected to V_{BB} (pin 11)
$Q_1 = G_1$; $Q_2 = \overline{G}_1$; $Q_3 = G_3$; $Q_4 = \overline{G}_3$; $Q_5 = G_5$; $Q_6 = \overline{G}_5$.

Positive logic:

H = HIGH state (the more positive voltage) = 1
L = LOW state (the less positive voltage) = 0

Fig. 4 Logic function.

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	27	25	27	mA	Pins 5,10,13 $V_I = V_{BB}$ Pins 4,9,12 $V_I = V_{BB}$
Input currents	I_{IHmax}	4*	180	115	115	μA	See Fig. 5 $V_I = V_{IHmax}$
	$ICBO_{max}$	4*	1,5	1,0	1,0	μA	See Fig. 5 $V_I = V_{EE}$
Reference voltage	V_{BB} min	11	−1 420	−1 350	−1 295	mV	See General spec "HOW TO TEST"
	V_{BB} max	11	−1 280	−1 230	−1 150	mV	

*Individually test each input applying the same mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	V_I at V_{IHmax}: (1)
		typ.		− 880		mV	invert output
		max.	− 890	− 810	− 700	mV	V_I at V_{ILmin} direct output
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	V_I at V_{ILmin}: (1)
		typ.		−1 720		mV	invert output
		max.	−1 675	−1 650	−1 615	mV	V_I at V_{IHmax} direct output
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	V_I at V_{IHC}: (1) invert output V_I at V_{ILC} direct output
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	V_I at V_{ILC}: (1) invert output V_I at V_{IHC} direct output

(1): See Fig. 5.

For common mode rejection test, use the same test configuration and limits as 10114 (Fig. 5).

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Propagation delay times	t_{PLH}/ t_{PHL}	min.	1,0	1,0	1,0	ns	For single-ended input, one input of each gate must be tied to V_{BB} (pin 11)
		typ.		1,5		ns	
		max.	2,6	2,5	2,8	ns	
Transition times rise and fall	t_{TLH}/ t_{THL}	min.	1,0	1,0	1,0	ns	
		typ.		1,5		ns	20% to 80%
		max.	2,6	2,5	2,8	ns	

For **switching time test circuit** and **waveforms** see Family Specifications.

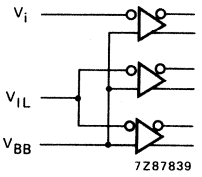


Fig. 5 Test circuit CMR test.

For common mode rejection tests use the same test configuration and limits as 10114.
Input under test V_I; The voltage on the other inputs are shifted 1 Volt CMR positive or negative,

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP

The 10231 is a high speed dual master slave D-type flip-flop. It contains asynchronous set (S) and reset (R) which override clock (C) and clock enable (C_E) inputs.
Each flip-flop may be clocked separately by using the enable inputs for the clocking function and holding the common clock in the LOW state. For the two flip-flops to be clocked, the common clock must be used with the clock enable inputs hold in the LOW state.
The outputs of the 10231 change state with the positive transition of the clock. Due to the master-slave structure of the device a change in the information present at the data (D) input will not modify the output information at any other time.
Unused inputs need not be tied to V_{EE} since input pull-down resistors are integrated in the circuit. All unused inputs must be tied to V_{IL} or V_{EE}.

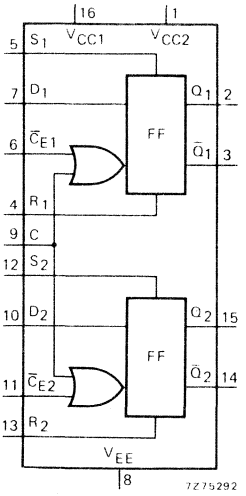


Fig. 1 Block diagram.

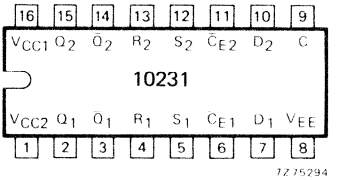


Fig. 2 Pin designation.

$V_{CC1} = V_{CC2} = 0$ V (ground);
$V_{EE} = -5{,}2$ V.

QUICK REFERENCE DATA

Supply voltage	V_{EE}		−5,2 V
Operating ambient temperature range	T_{amb}		−30 to +85 °C
Clock frequency	f_C	typ.	225 MHz
Output voltage			
HIGH state	V_{OH}	nom.	−880 mV
LOW state	V_{OL}	nom.	−1720 mV
Power consumption per package (no load)	P_D	typ.	270 mW

PACKAGE OUTLINES (see Package Outlines)

10231N: plastic 16-lead dual in-line (SOT-38).
10231F: ceramic 16-lead dual in-line (SOT-74).

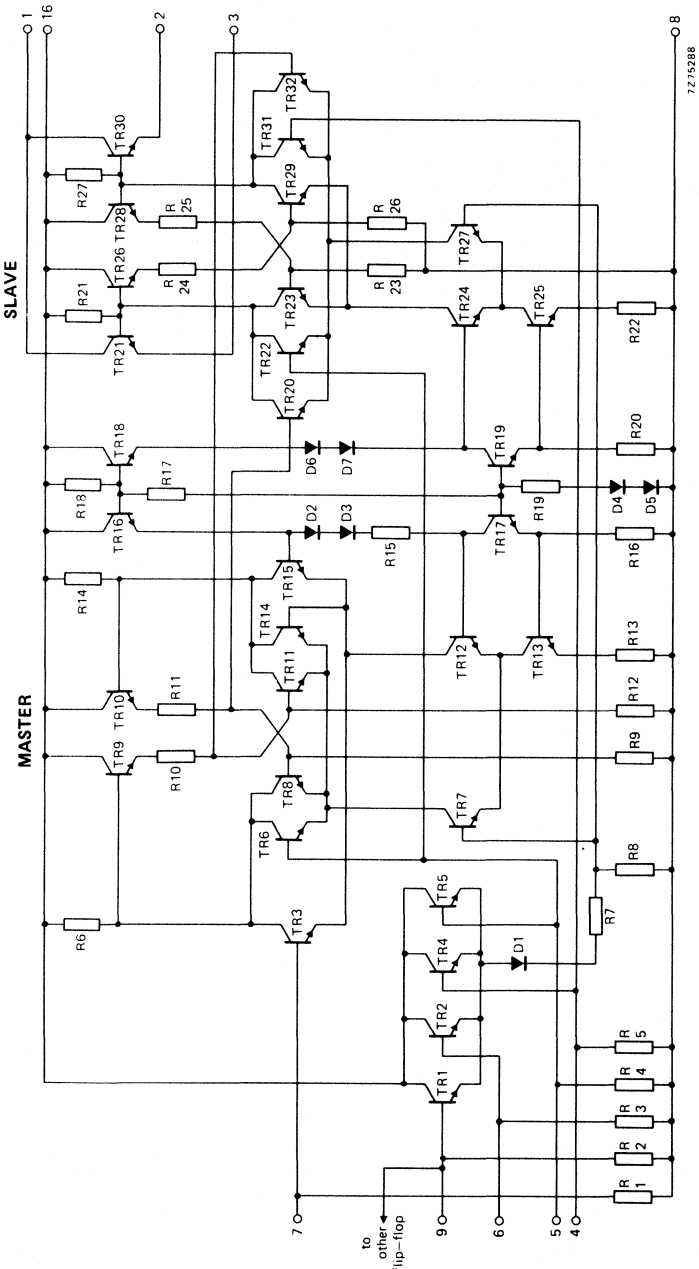


Fig. 3 Circuit diagram (one flip-flop).

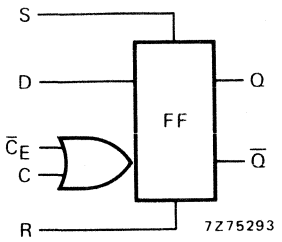


Fig. 4 Logic function.

C	D	Q_{n+1}**
L	X	Q_n
H	L	L
H	H	H

**R&S LOW

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	*

* Not allowed

Positive logic HIGH state = 1
LOW state = 0

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

For **switching times test circuit measurement of propagation** and **waveforms** see Family Specifications.

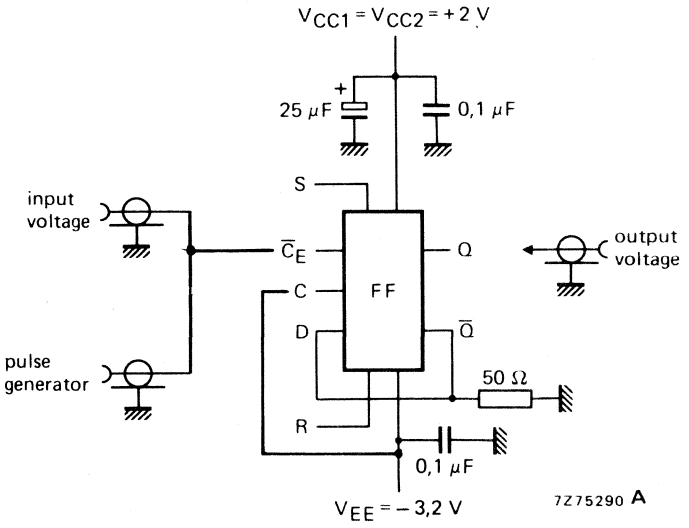


Fig. 5 Measurement of clock frequency.

D.C. CHARACTERISTICS

V_{CC} = 0 V (ground); V_{EE} = −5.2 V

	symbol	pin under test	T_{amb} (°C)			unit	conditions
			−30	+25	+85		
Supply current	I_{EEmax}	8	72	65	72	mA	
Input current LOW	I_{ILmin}	4*	0,5	0,5	0,3	μA	see "How to test Section"
Input current HIGH	I_{IHmax}	6,7,10,11	350	220	220	μA	
		9	460	290	290	μA	
		4,5,12,13	650	410	410	μA	

*Individually test each input applying the above mentioned conditions.

Output voltage HIGH	V_{OH}	min.	−1 060	− 960	− 890	mV	S at V_{IHmax} or R at V_{ILmin} D at V_{IHmax} CE at V_{ILmin} C at V_{IL} to V_{IH}
		typ.		− 880		mV	
		max.	− 890	− 810	− 700	mV	
Output voltage LOW	V_{OL}	min.	−1 890	−1 850	−1 825	mV	S at V_{ILmin} or R at V_{IHmax} D at V_{ILmin} CE at V_{ILmin} C at V_{IL} to V_{IH}
		typ.		−1 720		mV	
		max.	−1 675	−1 650	−1 615	mV	
Output threshold voltage HIGH	V_{OHC}	min.	−1 080	− 980	− 910	mV	S at V_{IHC} or R at V_{ILC} D at V_{IHC} CE at V_{ILC} C at V_{ILC} to V_{IHC}
Output threshold voltage LOW	V_{OLC}	max.	−1 655	−1 630	−1 595	mV	S at V_{ILC} or R at V_{IHC} D at V_{ILC} CE at V_{ILC} C at V_{ILC} to V_{IHC}

A.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2.0$ V; $V_{EE} = -3.2$ V; $R_L = 50\ \Omega$ to ground

	symbol	pin under test	T_{amb} (°C)			unit	remarks
			−30	+25	+85		
Rise and fall propagation delay times	t_{PLH} t_{PHL}						
C → Q		min.	1,5	1,5	1,6	ns	
		max.	3,4	3,3	3,7	ns	
S,R → Q		min.	1,1	1,1	1,2	ns	
		max.	3,4	3,3	3,7	ns	
Set-up time	t_s	min.	1,5	1,0	1,5	ns	
Hold time	t_h	min.	0,9	0,75	0,9	ns	
Clock frequency	f_C	min.	200	200	200	MHz	
Transition rise and fall times	t_{TLH} t_{THL}	min.	0,9	1,0	1,0	ns	between 20% and 80%
		max.	3,3	3,1	3,6	ns	

For switching times test circuit measurement of propagation and waveforms see Family Specifications.

FAMILY SPECIFICATIONS (ECL100 000)

FAMILY SPECIFICATIONS
ECL 100 000

These specifications cover the common electrical characteristics of the ECL100 000, unless otherwise specified in the individual device data sheet.

RATINGS: see chapter "MAXIMUM RATINGS"

D.C. CHARACTERISTICS at V_{CC} = ground; V_{EE} = −4,5 V

Each circuit has been designed to meet the d.c. specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed-circuit board and transverse air flow > 2,5 m/s is maintained. Test values are given in the table and defined in the figure.

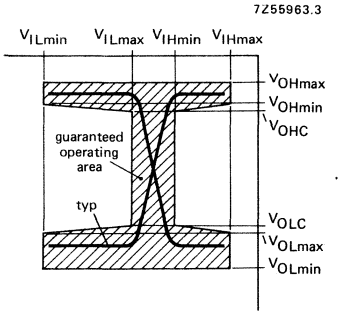


Fig. 1 Transfer characteristics.

D.C. characteristics $V_{CC1} = V_{CC2} = 0$ V (ground); $T_{amb} = 0$ to 85 °C; unless otherwise specified

$V_{EE} = -4{,}2$ V

description	symbol	min.	typ.	max.	unit	conditions
Output voltage HIGH	V_{OH}	−1025		−870	mV	$V_i = V_{IHmax}$ or V_{ILmin}*
Output threshold voltage HIGH	V_{OHC}	−1035			mV	$V_i = V_{IHmin}$ or V_{ILmax}*
Output threshold voltage LOW	V_{OLC}			−1590	mV	$V_i = V_{ILmax}$ or V_{IHmin}*
Output voltage LOW	V_{OL}	−1810		−1600	mV	$V_i = V_{ILmin}$ or V_{IHmax}*
Input voltage HIGH	V_{IH}	−1150		−880	mV	guaranteed HIGH signal for all inputs
Input voltage LOW	V_{IL}	−1810		−1475	mV	guaranteed LOW signal for all inputs

$V_{EE} = -4{,}5$ V

description	symbol	min.	typ.	max.	unit	conditions
Output voltage HIGH	V_{OH}	−1025	−955	−880	mV	$V_i = V_{IHmax}$ or V_{ILmin}*
Output threshold voltage HIGH	V_{OHC}	−1035			mV	$V_i = V_{IHmin}$ or V_{ILmax}*
Output threshold voltage LOW	V_{OLC}			−1610	mV	$V_i = V_{ILmax}$ or V_{IHmin}*
Output voltage LOW	V_{OL}	−1810	−1705	−1630	mV	$V_i = V_{ILmin}$ or V_{IHmax}*
Input voltage HIGH	V_{IH}	−1165		−880	mV	guaranteed HIGH signal for all inputs
Input voltage LOW	V_{IL}	−1810		−1475	mV	guaranteed LOW signal for all inputs

$V_{EE} = -4{,}8$ V

description	symbol	min.	typ.	max.	unit	conditions
Output voltage HIGH	V_{OH}	−1035		−880	mV	$V_i = V_{IHmax}$ or V_{ILmax}*
Output threshold voltage HIGH	V_{OHC}	−1045			mV	$V_i = V_{IHmin}$ or V_{ILmax}*
Output threshold voltage LOW	V_{OLC}			−1610	mV	$V_i = V_{ILmax}$ or V_{IHmax}*
Output voltage LOW	V_{OL}	−1830		−1620	mV	$V_i = V_{ILmin}$ or V_{IHmax}*
Input voltage HIGH	V_{IH}	−1165		−880	mV	guaranteed HIGH signal for all inputs
Input voltage LOW	V_{IL}	−1810		−1490	mV	guaranteed LOW signal for all inputs

* Loading with 50 Ω to −2,0 V.

A.C. CHARACTERISTICS

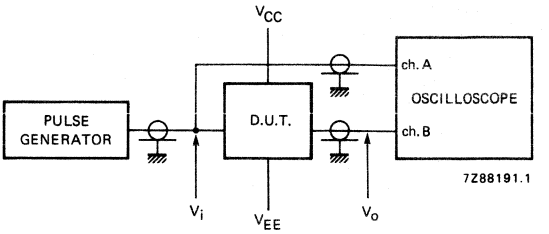


Fig. 2 Switching times test circuit. $V_{CC1} = V_{CC2} = +2{,}0$ V; $V_{EE} = -2{,}5$ V.

In order to test ECL100 000 circuits with a standard oscilloscope (load to ground), it is easier to use the test circuit with $V_{CC} = +2$ V, $V_{EE} = -2{,}5$ V and $R_L = 50\ \Omega$ to ground. All voltages given in the type specifications have then to be shifted by +2 V.

PROPAGATION DELAY

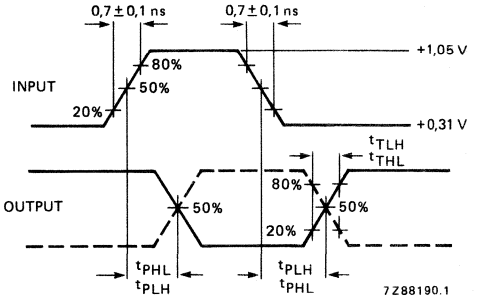


Fig. 3 Propagation delay waveform.

$V_{IH} = +1{,}05$ V; $V_{IL} = 0{,}31$ V

Notes

1. Input resistance is positive at any frequency.
2. In order to enable the output some circuits require application at HIGH level on other inputs. Refer to truth table in individual type specification.
3. Input and output cables to the oscilloscope are 50 Ω coaxial cables with equal length.
4. Input impedance of the oscilloscope has to be 50 Ω.
5. The unmatched wire stub between coaxial cable and pins under test must be less than 2 mm long for proper tests.
6. The propagation delay is measured at the leads of input and output 4 mm from the edge of the package (flatpack).

SET-UP TIME

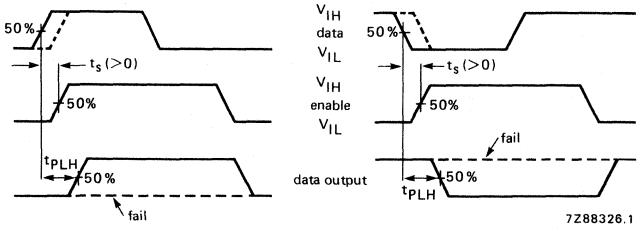


Fig. 4 Set-up time waveforms for rising and falling data signal (latch flip-flop).

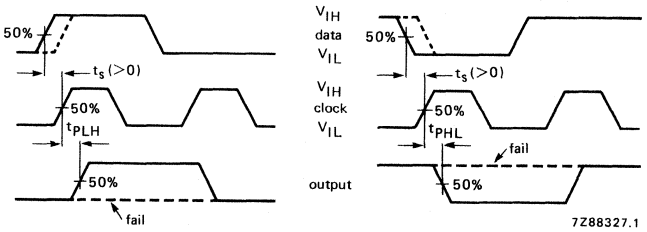


Fig. 5 Set-up time waveforms for rising and falling data signal (master-slave flip-flop).

Set up time (t_s) is the minimum time before the transition of the clock (or enable) that information must be present at the data input.

The limit value of set up time is positive if the transition of data signal is before the transition of clock (or enable) signal.

HOLD TIME

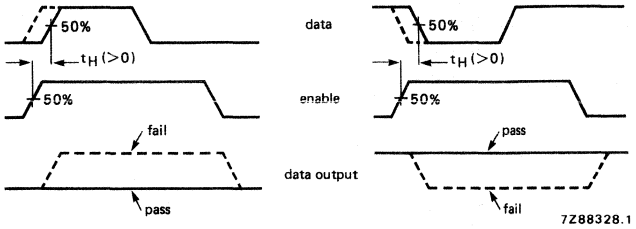


Fig. 6 Hold time waveforms for rising and falling data signal (latch flip-flop).

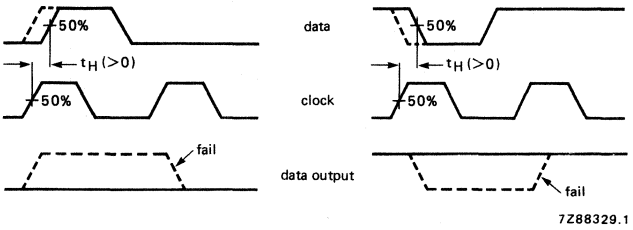


Fig. 7 Hold time waveforms for rising and falling data signal (master-slave flip-flop).

Hold time (t_h) is the minimum time after the transition of the clock (or enable) that information must remain unchanged at the data input.

The limit value of hold time is positive if the transition of data signal is after the transition of clock (or enable) signal.

RELEASE TIME

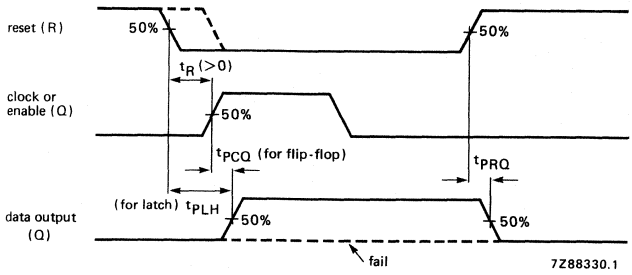


Fig. 8 Waveforms for release time (t_R). Reset; Data inputs are at HIGH level.

Release time (t_R) is the minimum time before the transition of the clock (or enable) that Reset must be suppressed.

The limit value of release time is positive if the transition of reset is before the transition of clock (or enable).

DEVICE DATA (ECL100 000)

TRIPLE 5-INPUT OR/NOR GATE

The device is a triple 5-input OR/NOR gate.
Each gate has an OR and a NOR output.

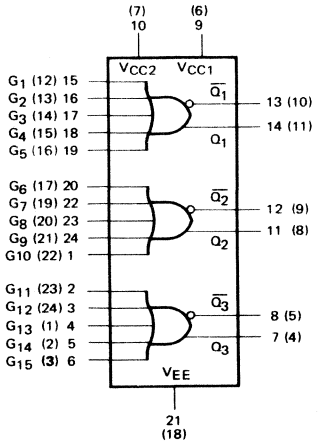


Fig. 1 Logic diagram.
Pin numbers of SLIM DIP package are between brackets

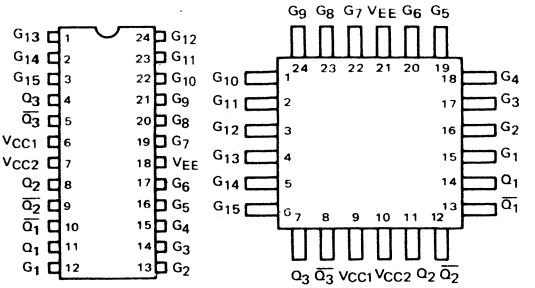


Fig. 2 Pin designation.
SLIM DIP and flat pack packages

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	0,75 ns
Power consumption per package	P_{av}	typ.	120 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100101Y: 24-lead flat-pack; ceramic (SOT-138).
100101F: 24-lead dual in-line; ceramic (cerdip) SOT-149).

TRUTH TABLE

INPUTS					OUTPUTS	
15(12) 20(17) 2(23)	16(13) 22(19) 3(24)	17(14) 23(20) 4(1)	18(15) 24(21) 5(2)	19(16) 1(22) 6(3)	13(10) 12(9) 8(5)	14(11) 11(8) 7(4)
L	L	L	L	L	H	H
H	x	x	x	x	L	H
x	H	x	x	x	L	H
x	x	H	x	x	L	H
x	x	x	H	x	L	H
x	x	x	x	H	L	H

Positive logic
1 = H = HIGH state (the more positive voltage)
0 = L = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

input current	symbol	min.	typ.	max.	unit	remarks
input current HIGH	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	18	27	38	nA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

CERAMIC DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,50	1,15	0,50	1,15	0,55	1,30	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,10	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,50	0,95	0,50	0,95	0,55	1,10	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,10	ns	

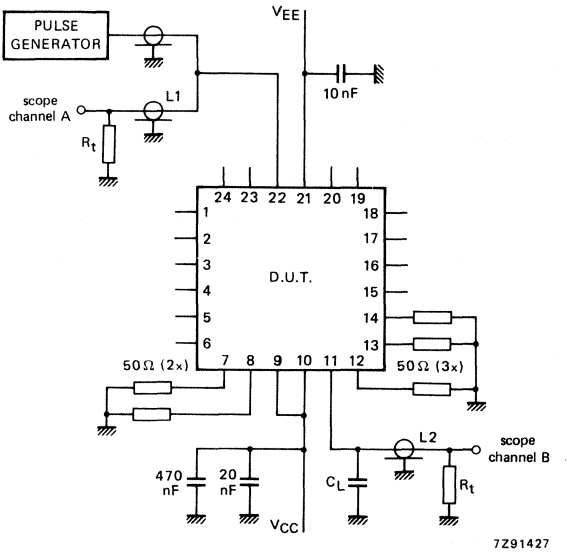


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V.
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT RACK. For dual in-line package see logic symbol.

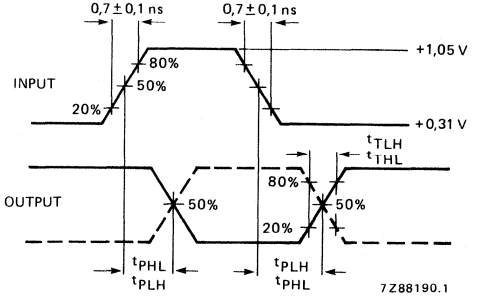


Fig. 4 Propagation delay and transition times waveforms

QUINTUPLE 2-INPUT OR/NOR GATE WITH COMMON ENABLE

The device has five 3-input gates. One input is a common enable to all five gates.

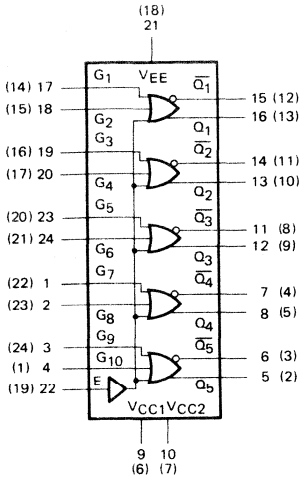


Fig. 1 Logic diagram.
Pin numbers of SLIM DIP package are between brackets.

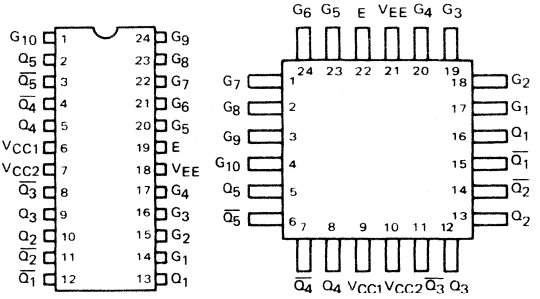


Fig. 2 Pin designation.
Slim dip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	0,75 ns
Power consumption per package	P_{av}	typ.	248 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100102Y: 24-lead flat-pack; ceramic (SOT-138).
100102F: 24-lead duel in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS			OUTPUTS	
4(1)	3(24)	22(19)	5(2)	6(3)
2(23)	1(22)	22(19)	8(5)	7(4)
24(21)	23(20)	22(19)	12(9)	11(8)
20(17)	19(16)	22(19)	13(10)	14(11)
18(15)	17(14)	22(19)	16(13)	15(12)
x	x	H	H	L
x	H	x	H	L
H	x	x	H	L
L	L	L	L	H

Positive logic
1 = H = HIGH state (the more positive voltage)
0 = L = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified,
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

input current	symbol	min.	typ.	max.	unit	remarks
input current HIGH data G	I_{IH}	–	–	350	μA	$V_{in} = V_{IH}$ max
enable E	I_{IH}	–	–	300	μA	$V_{in} = V_{IH}$max
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{IL}$min
supply current	$-I_{EE}$	38	55	80	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

CERAMIC DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,35	0,45	1,15	0,45	1,40	ns	
propagation delay E to OUTPUT	t_{PLH} t_{PHL}	0,90	2,15	0,95	2,15	0,95	2,20	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,10	ns	

FLATPACK

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,15	0,45	0,95	0,45	1,20	ns	
propagation delay E to OUTPUT	t_{PLH} t_{PHL}	0,90	1,95	0,95	1,95	0,95	2,00	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,10	ns	

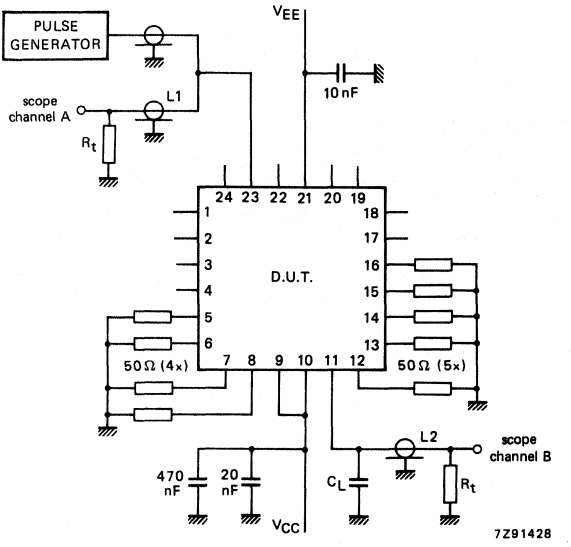


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines;
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

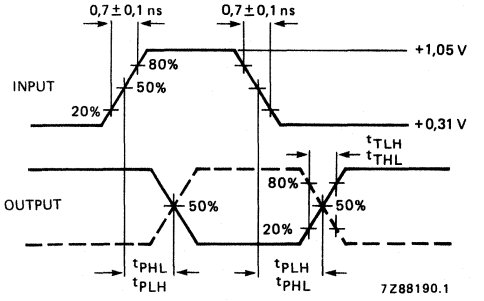


Fig. 4 Propagation delay and transition times waveforms.

QUINTUPLE EXCLUSIVE OR-NOR GATE WITH COMPARE

The device has five 2-input, 2-output exclusive OR-NOR gates with a compare output.

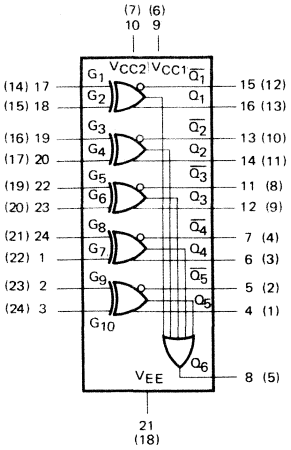


Fig. 1 Logic diagram.
Pin numbers of SLIM DIP package are between brackets

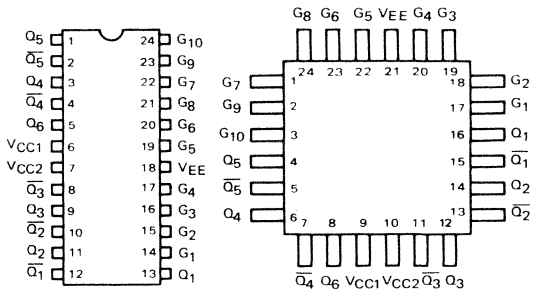


Fig. 2 Pin designation.
SLIM DIP and flat pack packages

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay DATA	t_{PLH}, t_{PHL}	typ.	0,95 ns
Power consumption per package	P_{av}	typ.	310 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100107Y: 24-lead flat-pack; ceramic (SOT-138).
100107F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS					OUTPUTS
17 ⊕ 18 (14⊕15)	19 ⊕ 20 (16⊕17)	22 ⊕ 23 (19⊕20)	24⊕1 (21⊕22)	2 ⊕ 3 (23⊕24)	8 (5)
L	L	L	L	L	L
H	x	x	x	x	H
x	H	x	x	x	H
x	x	H	x	x	H
x	x	x	H	x	H
x	x	x	x	H	H

INPUTS		OUTPUTS	
17(14) 19(16) 22(19) 24(21) 2(23)	18(15) 20(17) 23(20) 1(22) 3(24)	16(13) 14(11) 12(9) 6(3) 4(1)	15(12) 13(10) 11(8) 7(4) 5(2)
L	L	L	H
L	H	H	L
H	L	H	L
H	H	L	H

⊕ = exclusive OR

Positive logic
1 = H = HIGH state (the more positive voltage)
0 = L = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

input current	symbol	min.	typ.	max.	unit	remarks
input current HIGH						
even inputs (G2-G10)	I_{IH}	–	–	250	μA	$V_{in} = V_{IHmax}$
odd inputs (G1-G9)	I_{IH}	–	–	350	μA	
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	46	68	96	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL-IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay									
G_n to OUTPUT									
even inputs (G2-G10)	t_{PLH} / t_{PHL}	0,55	1,90	0,55	1,80	0,55	1,90	ns	see Figs 3 and 4
odd inputs (G1-G9)	t_{PLH} / t_{PHL}	0,55	1,70	0,55	1,60	0,55	1,70	ns	
DATA G_n to COMPARE	t_{PLH} / t_{PHL}	1,15	2,75	1,15	2,75	1,15	3,00	ns	
transition time	t_{TLH} / t_{THL}	0,45	1,70	0,45	1,55	0,45	1,70	ns	

FLATPACK

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay									
G_n to OUTPUT									
even inputs (G1-G10)	t_{PLH} / t_{PHL}	0,55	1,70	0,55	1,60	0,55	1,70	ns	
odd inputs (G1-G9)	t_{PLH} / t_{PHL}	0,55	1,50	0,55	1,40	0,55	1,50	ns	see Figs 3 and 4
DATA G_n to COMPARE	t_{PLH} / t_{PHL}	1,15	2,55	1,15	2,55	1,15	2,80	ns	
transition time	t_{TLH} / t_{THL}	0,45	1,70	0,45	1,55	0,45	1,70	ns	

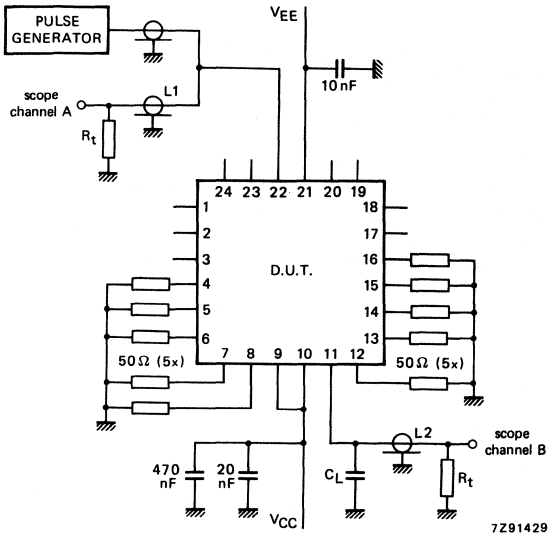


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length; 50 Ω impedance lines;
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and straly capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

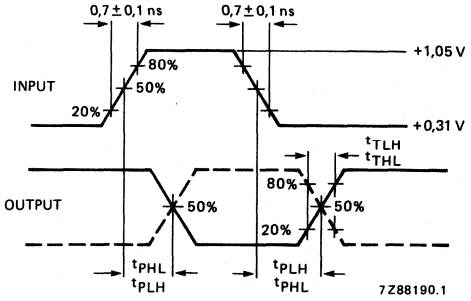


Fig. 4 Propagation delay and transition times waveforms

QUADRUPLE DOUBLE FAN-OUT OR/NOR GATE

The device has four 2-input OR/NOR gates with one common input.
Each gate has two OR outputs and two NOR outputs.

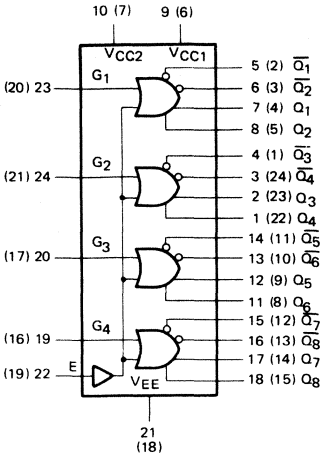


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP are between brackets.

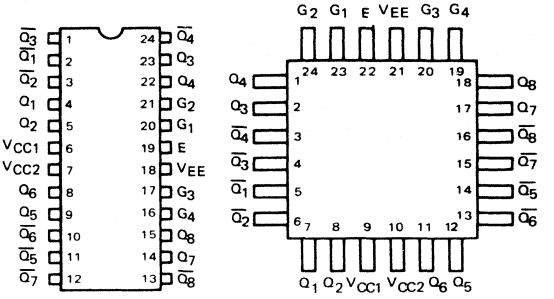


Fig. 2 Pin designation.
Slim cerdip and flat pack packages

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	0,85 ns
Average propagation delay (input 22)	t_{PLH}, t_{PHL}	typ.	1,40 ns
Power consumption per package	P_{av}	typ.	330 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100112Y: 24-lead flat-pack; ceramic (SOT-138).
100112F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS		OUTPUTS			
19(16) 20(17) 23(20) 24(21)	22(19) 22(19) 22(19) 22(19)	15(12) 14(11) 5(2) 4(1)	16(13) 13(10) 6(3) 3(24)	17(14) 12(9) 7(4) 2(23)	18(15) 11(8) 8(5) 1(22)
H	x	L	L	H	H
x	H	L	L	H	H
L	L	H	H	L	L

Positve logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

input current	symbol	min.	typ.	max.	unit	remarks
input current HIGH DATA G_n	I_{IH}	–	–	550	μA	$V_{in} = V_{IHmax}$
ENABLE E	I_{IH}	–	–	450	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	51	73	106	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,55	1,50	0,55	1,40	0,45	1,60	ns	
E to OUTPUT	t_{PLH} t_{PHL}	0,65	2,00	0,65	1,90	0,65	2,00	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,55	1,30	0,55	1,20	0,45	1,40	ns	
E to OUTPUT	t_{PLH} t_{PHL}	0,65	1,80	0,65	1,70	0,65	1,80	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

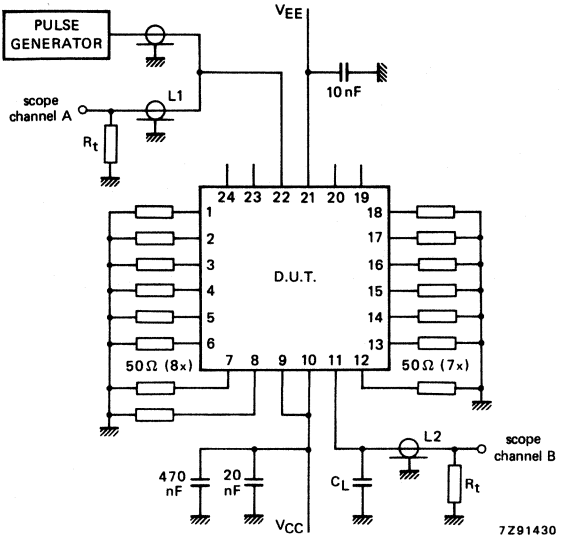


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
$R_t = 50$ Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

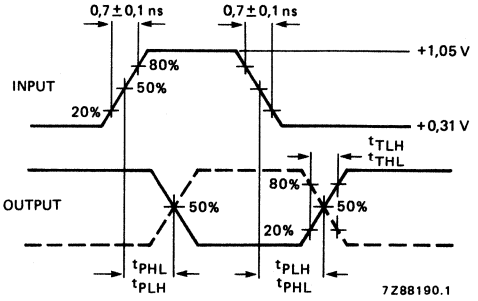


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

QUADRUPLE DOUBLE FAN-OUT OR/NOR GATE

The device has four 2-input OR/NOR gates with one common input.
Each gate has two OR outputs and two NOR outputs.

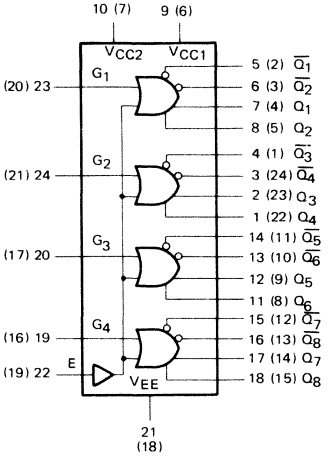


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

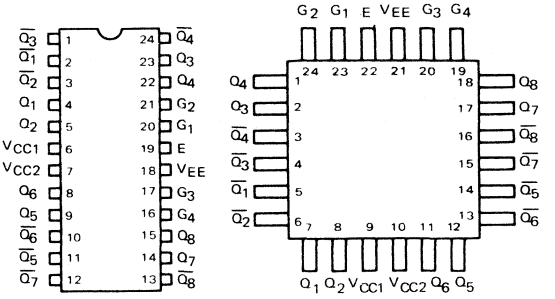


Fig. 2 Pin designation.
Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	0,80 ns
Average propagation delay (input 22)	t_{PLH}, t_{PHL}	typ.	1,40 ns
Power consumption per package	P_{av}	typ.	340 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100113Y: 24-lead flat-pack; ceramic (SOT-138).
100113F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS		OUTPUTS			
19(16) 20(17) 23(20) 24(21)	22(19) 22(19) 22(19) 22(19)	15(12) 14(11) 5(2) 4(1)	16(13) 13(10 6(3) 3(24)	17(14) 12(9) 7(4) 2(23)	18(15) 11(8) 8(5) 1(22)
H	x	L	L	H	H
x	H	L	L	H	H
L	L	H	H	L	L

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

input current	symbol	min.	typ.	max.	unit	remarks
input current HIGH DATA G_n	I_{IH}	–	–	550	μA	$V_{in} = V_{IHmax}$
ENABLE E	I_{IH}	–	–	450	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	54	75	116	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,40	0,45	1,35	0,45	1,40	ns	
E to OUTPUT	t_{PLH} t_{PHL}	0,55	1,90	0,55	1,90	0,55	1,90	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

FLATPACK

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,20	0,45	1,15	0,45	1,20	ns	
E to OUTPUT	t_{PLH} t_{PHL}	0,55	1,70	0,55	1,70	0,55	1,70	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

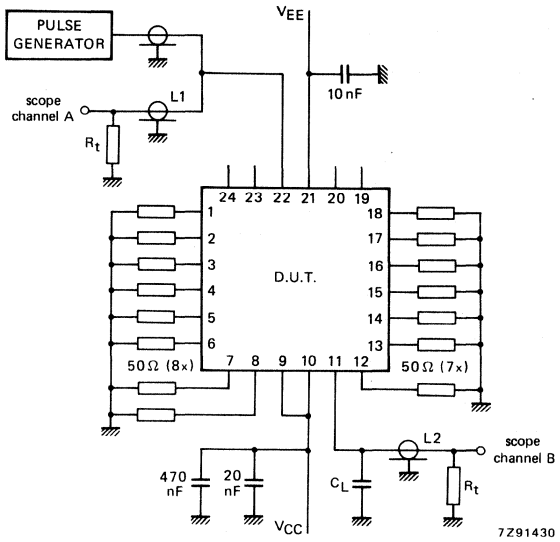


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines;
$R_t = 50$ Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

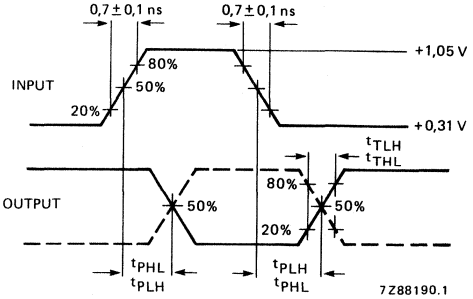


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

QUINTUPLE DIFFERENTIAL LINE RECEIVER

The device contains five gates with differential inputs and complementary outputs. An internal reference is available (V_{BB}), which enables, when connected to a gate input, the other to operate as a standard 100K ECL input. The direct output of a gate goes LOW and the complementary goes HIGH, when both inputs are either open or at V_{CC} or have equal voltage applied.

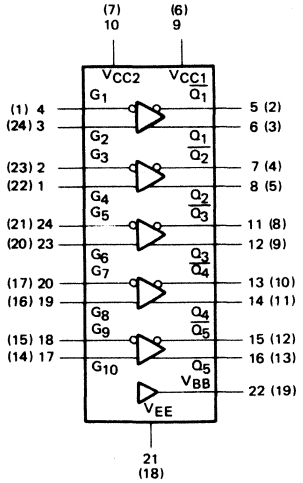


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

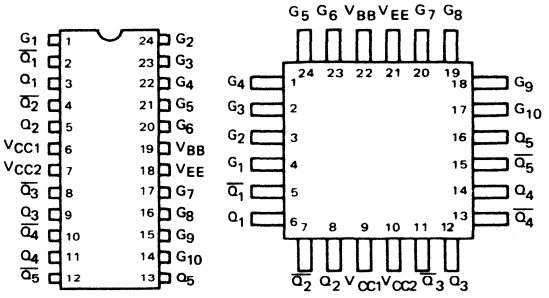


Fig. 2 Pin designation.
Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	1,40 ns
Power consumption per package	P_{av}	typ.	330 mW
Operating HIGH input voltage range	V_{IH}		−2,15 to −0,23 V

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100114Y: 24-lead flat-pack; ceramic (SOT-138).
100114F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS		OUTPUTS	
18(15) 20(17) 24(21) 2(23) 4(1)	17(14) 19(16) 23(20) 1(22) 3(24)	15(12) 13(10) 11(8) 7(4) 5(2)	16(13) 14(11) 12(9) 8(5) 6(3)
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$V_{ID} \geqslant 0V$		H	L
$V_{ID} \leqslant -0{,}15V$		L	H
$-0{,}15V < V_{ID} < 0V$		*	*
open	open	H	L
V_{CC}	V_{CC}	H	L

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
* = indeterminate state
V_{BB} = internal reference voltage (pin 22 (18))
V_{ID} = complement to direct input voltage difference

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH	I_{IH}	–	–	65	μA	$V_{in} = V_{IHmax}$ second input to V_{BB} or open
input leakage current	I_{CBO}	–10	–	–	μA	$V_{in} = V_{EE}$ second input to V_{BB}
supply current	$-I_{EE}$	51	73	106	mA	all complement inputs to V_{ILmin} and all direct inputs to V_{BB}
input voltage HIGH	$V_{IH}max$	–	–	–230	mV	
external input reference voltage	V_{REF}	–2,3	–	–	V	
common mode voltage	V_{CM}	–	–	1,0	V	permissible ± V_{CM} with respect to V_{BB}
differential input voltage	V_{diff}	150	–	–	mV	required for full output swing
reference voltage output (I_{BB} = 0 to 475 μA)	V_{BB} V_{BB}	–1380 –1396	–1320 –1320	–1260 –1244	mV mV	V_{EE} = –4,5 V V_{EE} = –4,2 to 4,8 V

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,55	2,20	0,60	2,20	0,70	2,40	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,30	0,45	1,20	0,45	1,30	ns	

FLATPACK

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,55	2,00	0,60	2,00	0,70	2,20	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,30	0,45	1,20	0,45	1,30	ns	

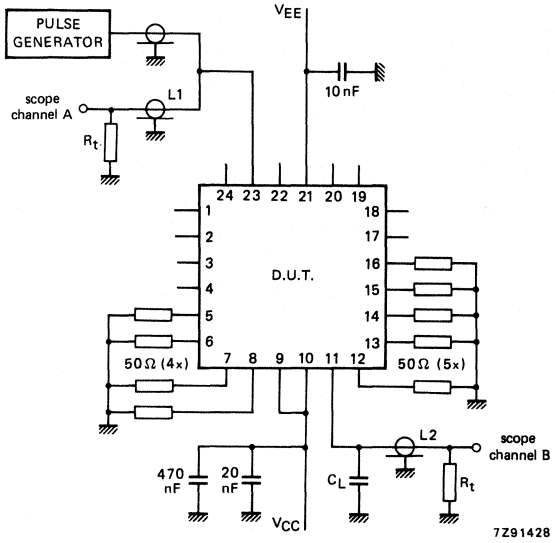


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines;
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

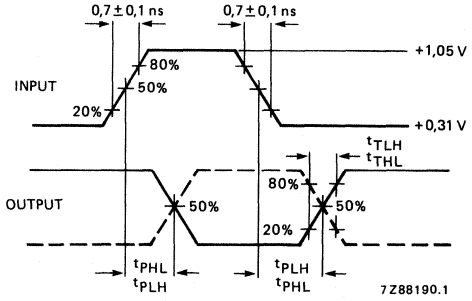


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

TRIPLE 1-2-2 INPUT OR/AND, OR/NAND GATE

The device has three 1-2-2 input OR/NAND gates with direct and complement output.

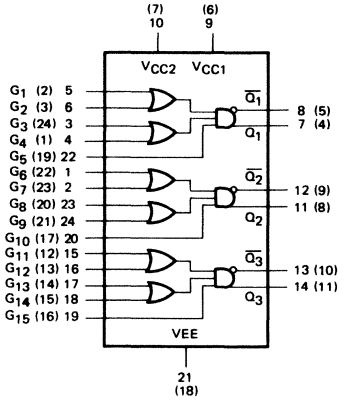


Fig. 1 Logic diagram
Pin numbers of SLIM CERDIP package are between brackets.

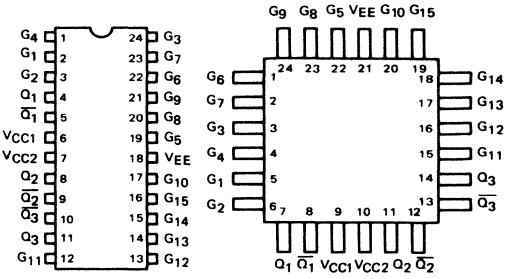


Fig. 2 Pin designation.
Slim cerdip and flat packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay			
DATA G	t_{PLH},t_{PHL}	typ.	1,40 ns
ENABLE G ($G_{5,10,15}$)	t_{PLH},t_{PHL}	typ.	0,75 ns
Power consumption per package	P_{av}	typ.	255 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100117Y: 24-lead flat-pack; ceramic (SOT-138).
100117F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS					OUTPUTS	
19(16) 20(17) 22(19)	15(12) 23(20) 3(24)	16(13) 24(21) 4(1)	17(14) 1(22) 5(2)	18(15) 2(23) 6(3)	13(10) 12(9) 8(5)	14(11) 11(8) 7(4)
L	x	x	x	x	H	L
x	L	L	x	x	H	L
x	x	x	L	L	H	L
H	H	x	H	x	L	H
H	x	H	x	H	L	H
H	H	x	x	H	L	H
H	x	H	H	x	L	H

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH DATA G inputs	I_{IH}	–	–	220	μA	$V_{in} = V_{IHmax}$
G ENABLE inputs ($G_{5,10,15}$)	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	37	57	79	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay DATA G to Q	t_{PLH} t_{PHL}	0,90	2,60	0,90	2,50	0,90	2,60	ns	
ENABLE G to Q ($G_{5,10,15}$)	t_{PLH} t_{PHL}	0,45	1,40	0,45	1,30	0,45	1,40	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,20	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay DATA G to Q	t_{PLH} t_{PHL}	0,90	2,40	0,90	2,30	0,90	2,40	ns	
ENABLE G to Q ($G_{5,10,15}$)	t_{PLH} t_{PHL}	0,45	1,20	0,45	1,10	0,45	1,20	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,20	0,45	1,10	0,45	1,20	ns	

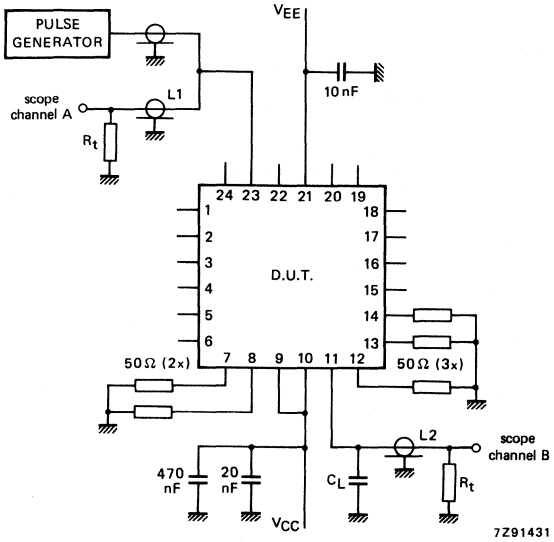


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

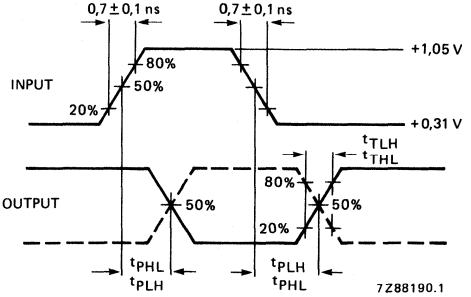
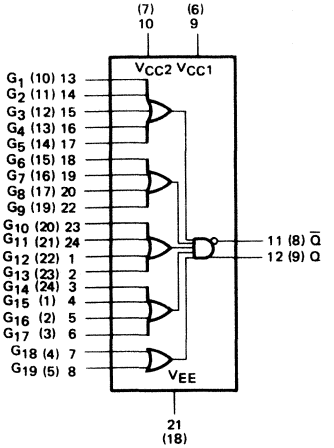


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

2-4-4-4-5 INPUT OR/AND, OR/NAND GATE

The device has one 2-4-4-4-5 input OR/NAND gate with direct and complement output.



Logic 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

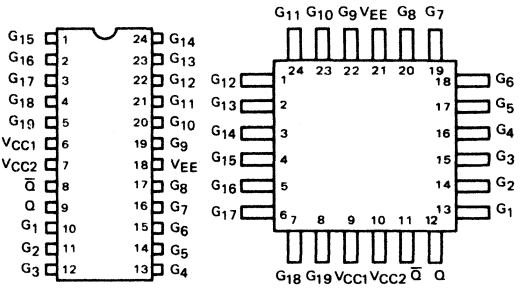


Fig. 2 Pin designation.
Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	1,15 ns
Power consumption per package	P_{av}	typ.	195 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100118Y: 24-lead flat-pack; ceramic (SOT-138).
100118F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS																		OUTPUTS	
13 (10)	14 (11)	15 (12)	16 (13)	17 (14)	18 (15)	19 (16)	20 (17)	22 (19)	23 (20)	24 (21)	1 (22)	2 (23)	3 (24)	4 (1)	5 (2)	6 (3)	7 (4)	8 (5)	11 (8)	12 (9)
L	L	L	L	L	x	x	x	x	x	x	x	x	x	x	x	x	x	x	H	L
x	x	x	x	x	L	L	L	L	x	x	x	x	x	x	x	x	x	x	H	L
x	x	x	x	x	x	x	x	x	L	L	L	L	x	x	x	x	x	x	H	L
x	x	x	x	x	x	x	x	x	x	x	x	x	L	L	L	L	x	x	H	L
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	L	L	H	L
other configurations																			L	H

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	32	43	92	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,85	3,20	0,85	3,20	0,85	3,40	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,85	3,00	0,85	3,00	0,85	3,20	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,40	0,45	1,50	ns	

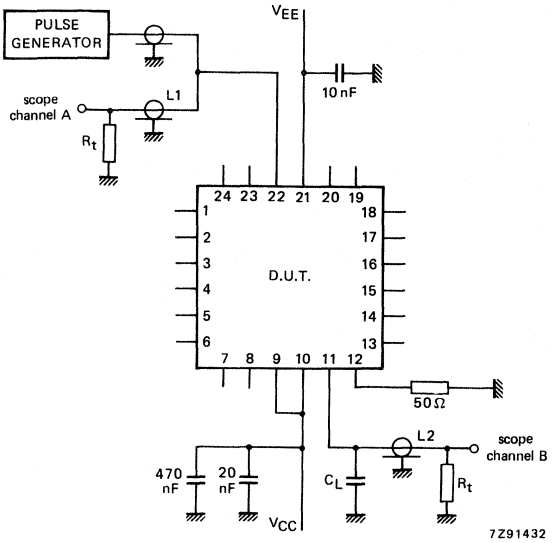


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
$R_t = 50$ Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

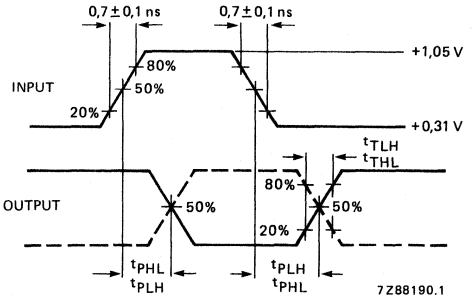


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

9 GATE BUFFER

The device contains 9 buffer gates.

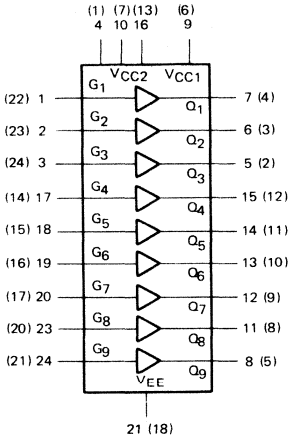


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

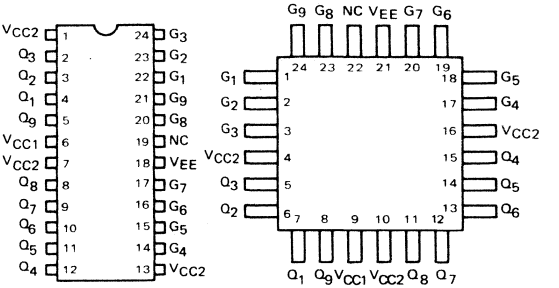


Fig. 2 Pin designation
Slim cerdip and flat pack packages

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	0,75 ns
Power consumption per package	P_{av}	typ.	350 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100122Y: 24-lead flat-pack; ceramic (SOT-138).
100122F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

RATINGS see Familiy Specifications.

D.C. CHARACTERSITICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	46	78	96	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,60	0,45	1,45	0,45	1,60	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,30	0,45	1,30	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	0,45	1,40	0,45	1,25	0,45	1,40	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,30	0,45	1,30	ns	

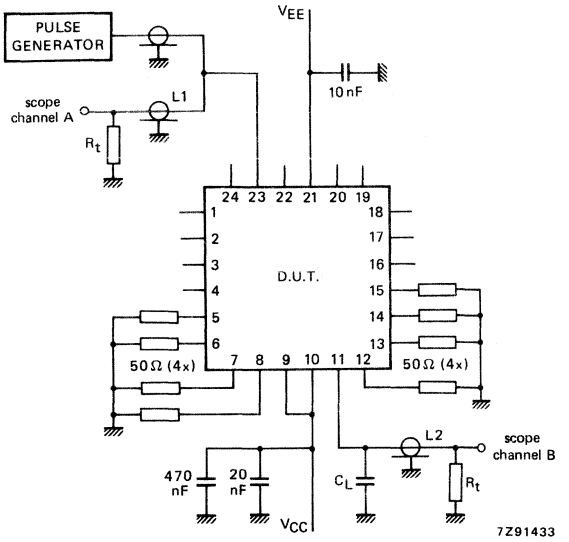


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

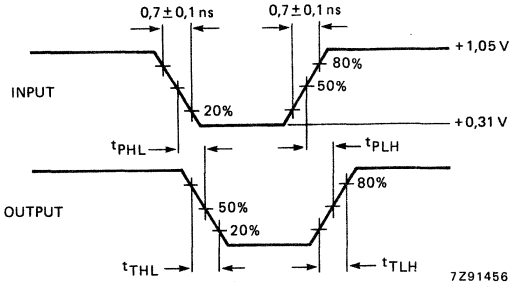


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

HEX BUS DRIVER

The device contains six bus drivers capable of driving terminated lines with terminations as low as 25 Ω. Each output has its respective ground connection. The driver itself performs the positive logic AND of a data input and the OR of two enable inputs.
The output voltage low level is more negative than usual ECL outputs. This allows an emitter-follower output transistor to turn off, when the termination supply V_T is −2,0 ± 0,2 V.

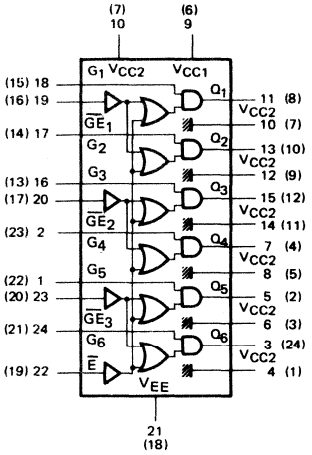


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

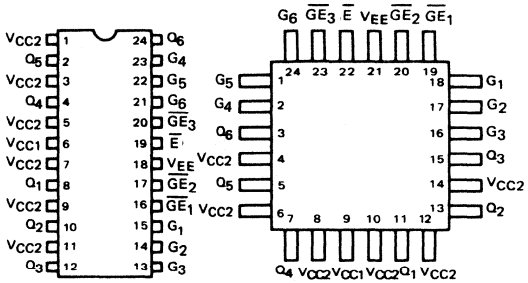


Fig. 2 Pin designation.
Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Output voltage LOW (depending on V_T)	V_{OL}	max.	−2,20 V
Power consumption per package	P_{av}	typ.	730 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100123Y: 24-lead flat-pack; ceramic (SOT-138).
100123F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUT			OUTPUT
22(19)	23(20	24(21)	3(24)
22(19)	23(20)	1(22)	5(2)
22(19)	20(17)	2(23)	7(4)
22(19)	20(17)	16(13)	15(12)
22(19)	19(16)	17(14)	13(10)
22(19)	19(16)	18(15)	11(8)
x	x	L	L
L	L	H	L
H	x	H	H
x	H	H	H

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH						
common $\overline{E}$	I_{IH}	–	–	330	μA	$V_{in} = V_{IHmax}$
G_n and $\overline{GE}_n$	I_{IH}	–	–	260	μA	
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
output voltage*						
HIGH	V_{OH}	–1025	–955	– 880	mV	V_{EE} = –4,5 V
HIGH	V_{OH}	–1035	–	– 870	mV	V_{EE} = –4.2 to –4.8 V
LOW	V_{OL}	–	–	–2200	mV	loaded with 25 Ω to –2,3 V
output threshold voltage*						
HIGH	V_{OHC}	–1035	–	–	mV	V_{EE} = –4,5 V
HIGH	V_{OHC}	–1045	–	–	mV	V_{EE} = –4,2 to –4,8 V
supply current	$-I_{EE}$	113	176	235	mA	inputs open

*Loaded with 25 Ω to –2,0 V.

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground; outputs loaded with 25 Ohm.

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay	t_{PLH}	1,70	4,35	1,75	4,35	1,75	4,65	ns	see Figs 3 and 4
G_n to OUTPUT	t_{PHL}	1,00	2,40	1,00	2,40	1,10	2,60	ns	
$\overline{GE}_n$ to OUTPUT	t_{PLH}	2,00	4,70	2,00	4,70	2,00	5,10	ns	
	t_{PHL}	1,20	3,00	1,20	3,00	1,20	3,40	ns	
$\overline{E}$ to OUTPUT	t_{PLH}	2,10	5,40	2,10	5,30	2,10	5,80	ns	
	t_{PHL}	1,20	3,30	1,20	3,30	1,20	3,70	ns	
transition time	t_{TLH}	0,70	2,00	0,70	1,90	0,70	2,10	ns	
	t_{THL}	0,45	1,30	0,45	1,20	0,45	1,30	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay	t_{PLH}	1,70	4,15	1,75	4,15	1,75	4,45	ns	see Figs 3 and 4
G_n to OUTPUT	t_{PHL}	1,00	2,20	1,00	2,20	1,10	2,40	ns	
$\overline{GE}_n$ to OUTPUT	t_{PHL}	2,00	4,50	2,00	4,50	2,00	4,90	ns	
	t_{PHL}	1,20	2,80	1,20	2,80	1,20	3,20	ns	
$\overline{E}$ to OUTPUT	t_{PLH}	2,10	5,20	2,10	5,10	2,10	5,60	ns	
	t_{PHL}	1,20	3,10	1,20	3,10	1,20	3,50	ns	
transition time	t_{TLH}	0,70	2,00	0,70	1,90	0,70	2,10	ns	
	t_{THL}	0,45	1,30	0,45	1,20	0,45	1,30	ns	

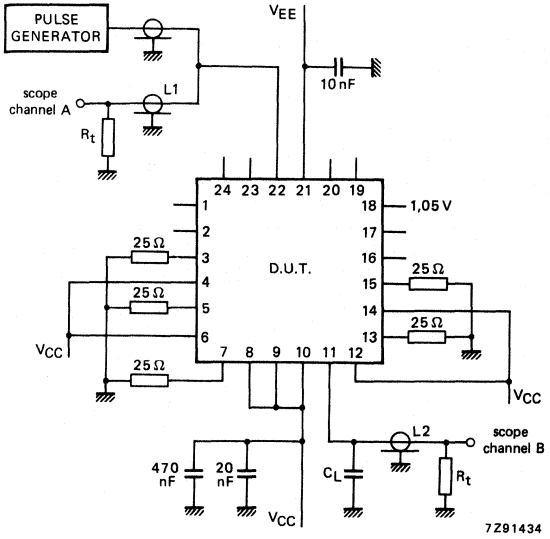


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 25 Ω impedance lines.
R_t = 25 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 25 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

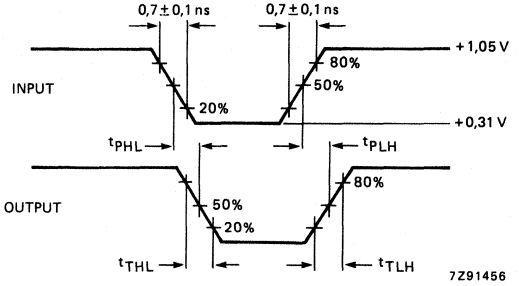


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

9 GATE BUFFER

The device contains 9 buffer gates.

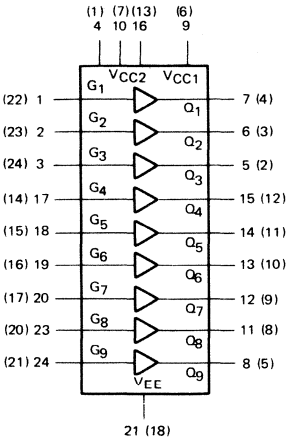


Fig. 1 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

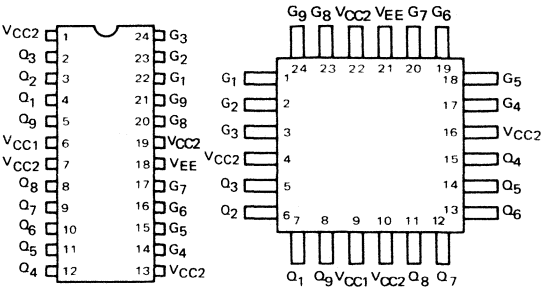


Fig. 2 Pin designation.
Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	typ.	2,0 ns
Power consumption per package	P_{av}	typ.	350 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100126Y: 24-lead flat-pack; ceramic (SOT-138).
100126F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	46	78	96	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	1,05	2,75	1,05	2,75	1,05	2,75	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	1,15	3,30	1,15	3,30	1,05	3,30	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay G_n to OUTPUT	t_{PLH} t_{PHL}	1,05	2,55	1,05	2,55	1,05	2,55	ns	see Figs 3 and 4
transition time	t_{TLH} t_{THL}	1,15	3,30	1,15	3,30	1,05	3,30	ns	

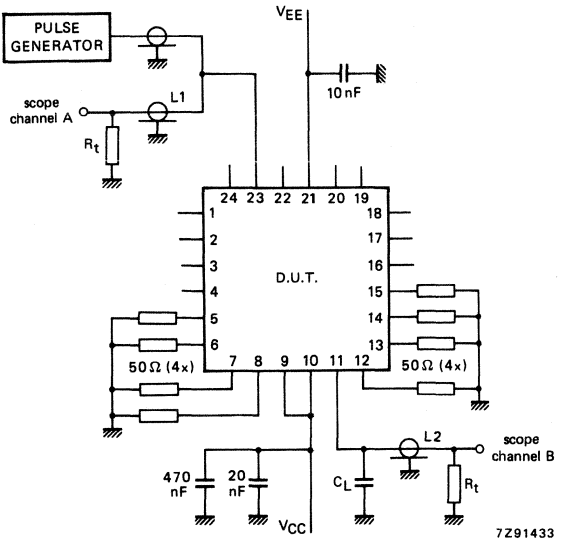


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

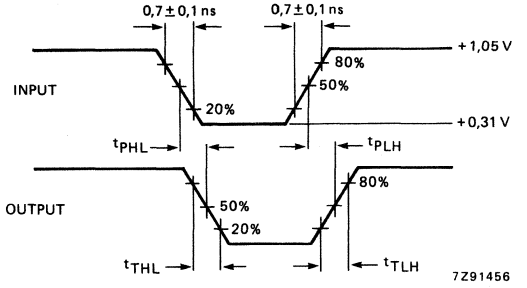


Fig. 4 Propagation delay and transition times waveforms.
(rise and fall times)

TRIPLE D-TYPE MASTER-SLAVE FLIP-FLOP

The device has three D-type master-slave flip-flops with direct and complement outputs, separate clock, set and reset.
In additon, all three flip-flops have a common clock, set and reset.

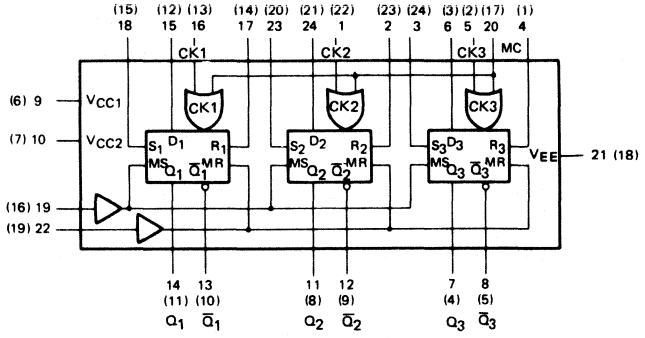


Fig. 1 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

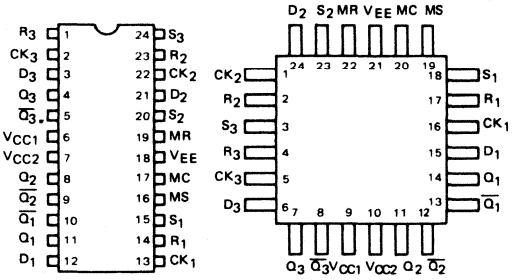


Fig. 2 Pin designation. Slim cerdip and flat packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ. −4,5 V
Operating ambient temperature	T_{amb}	0 to +85 °C
Average propagation delay	t_{PLH}, t_{PHL}	1,3 ns
Power consumption per package	P_{av}	495 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100131Y: 24-lead flat-pack; ceramic (SOT-138).
100131F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS							OUTPUTS	
D_i	MC	CK_i	MS	S_i	MR	R_i	Q_{n+1}	$\overline{Q_{n+1}}$
15(12) 24(21) 6(3)	20(17) 20(17) 20(17)	16(13) 1(22) 5(2)	19(16) 19(16) 19(16)	18(15) 23(20 3(24)	22(19) 22(19) 22(19)	17(14) 2(23) 4(1)	14(11) 11(8) 7(4)	13(10) 12(9) 8(5)
x	x	x	L	L	H	x	L	H
x	x	x	L	L	x	H	L	H
x	x	x	H	x	L	L	H	L
x	x	x	x	H	L	L	H	L
x	x	x	H	x	H	x	*	*
x	x	x	H	x	x	H	*	*
x	x	x	x	H	H	x	*	*
x	x	x	x	H	x	H	*	*
x	x	⌐	L	L	L	L	Q_n	Q_n
x	⌐	H	L	L	L	L	Q_n	Q_n
x	x	x	L	L	L	L	Q_n	Q_n
H	⌐	L	L	L	L	L	H	L
L	⌐	L	L	L	L	L	L	H
H	L	⌐	L	L	L	L	H	L
L	L	⌐	L	L	L	L	L	H

D_i = Data input
MS = Master Set
R_i = Reset
n = state before transition
MC = Master Clock
S_i = Set input
Q = direct output
n+1 = state after transition
CK_i = Clock
MR = Master Reset
$\overline{Q}$ = Complement output
⌐ = LOW or HIGH transition

DATA enters a master, when both CLOCK and MASTER CLOCK are LOW, and transfers to the slave, when the CLOCK or MASTER CLOCK (or both) go HIGH. If the SET (or MASTER SET) is HIGH while the RESET (or MASTER RESET) is HIGH, the output is indefined.

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)
* = output is indefined

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8, V; unless otherwise specified; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current HIGH						
D_i, CK_i	I_{IH}	–	–	240	μA	$V_{in} = V_{IHmax}$
MC, MS, MR	I_{IH}	–	–	450	μA	
R_i, S_i	I_{IH}	–	–	530	μA	
input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	74	110	149	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay									
MC to OUTPUT	t_{PLH} t_{PHL}	0,75	2,40	0,75	2,15	0,70	2,30	ns	see Figs 3 and 5
CK_i to output	t_{PLH} t_{PHL}	0,70	2,20	0,70	2,00	0,70	2,20	ns	
MR, MS to output									
MC, CK; LOW	t_{PLH} t_{PHL}	1,10	2,70	1,05	2,60	1,05	2,70	ns	
MC, CK; HIGH	t_{PLH} t_{PHL}	1,05	3,05	1,05	2,95	1,05	3,05	ns	see Figs 3 and 6
R, S to output									
MC, CK; LOW	t_{PLH} t_{PHL}	0,65	1,90	0,70	1,70	0,70	1,90	ns	
MC, CK; HIGH	t_{PLH} t_{PHL}	0,70	2,10	0,70	2,00	0,70	2,20	ns	
transition time	t_{TLH} t_{THL}	0,45	2,00	0,45	1,60	0,45	1,70	ns	see Figs
set-up time data	t_s	0,90	–	0,70	–	0,90	–	ns	see Fig. 7
hold time data	t_h	0,60	–	0,60	–	0,80	–	ns	see Fig. 7
release time									
R and S	t_r	1,50	–	1,30	–	1,50	–	ns	see Fig. 7
MR and MS	t_r	2,50	–	2,30	–	2,50	–	ns	
toggle freq.	f_{max}	325	–	325	–	325	–	MHz	see Figs
Pulsewidth HIGH									
MC,MR,MS,CK R and S	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Figs

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
propagation delay MC to OUTPUT	t_{PLH} t_{PHL}	0,75	2,20	0,75	1,95	0,70	2,10	ns	see Figs 3 and 5
CK_n to output	t_{PLH} t_{PHL}	0,70	2,00	0,70	1,80	0,70	2,00	ns	
MR,MS to output MC, CK; LOW	t_{PLH} t_{PHL}	1,10	2,50	1,05	2,40	1,05	2,50	ns	
MC, CK; HIGH	t_{PLH} t_{PHL}	1,05	2,85	1,05	2,75	1,05	2,85	ns	see Figs 3 and 6
R, S to output MC, CK; LOW	t_{PLH} t_{PHL}	0,65	1,70	0,70	1,50	0,70	1,70	ns	
MC, CK; HIGH	t_{PLH} t_{PHL}	0,70	1,90	0,70	1,80	0,70	2,00	ns	
transition time	t_{TLH} t_{THL}	0,45	2,00	0,45	1,60	0,45	1,70	ns	see Figs 3,5&6
set-up time data	t_s	0,80	–	0,60	–	0,80	–	ns	see Fig. 7
hold time data	t_h	0,50	–	0,50	–	0,70	–	ns	see Fig. 7
release time R and S	t_r	1,40	–	1,20	–	1,40	–	ns	see Fig. 6
release time MR, MS	t_r	2,40	–	2,20	–	2,40	–	ns	see Fig. 6
toggle freq.	f_{max}	350	–	350	–	350	–	MHz	see Figs 4 and 5
pulsewidth HIGH MC,MR,MS,CK R and S	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Figs 5 and 6

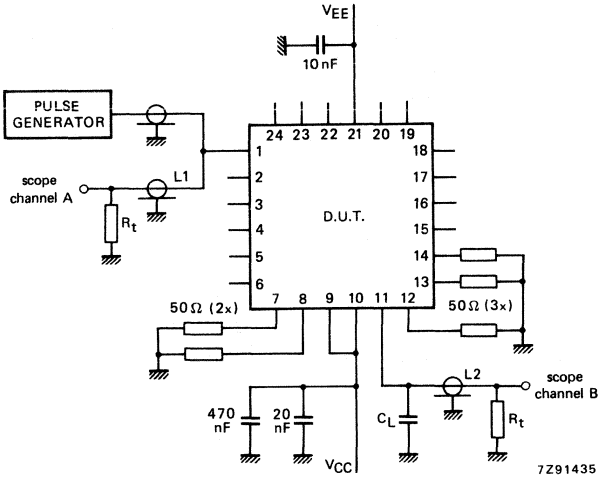


Fig. 3 Switching time test circuit

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length. 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

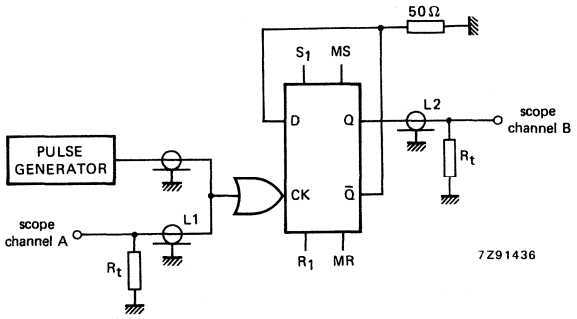


Fig. 4 Toggle frequency test circuit

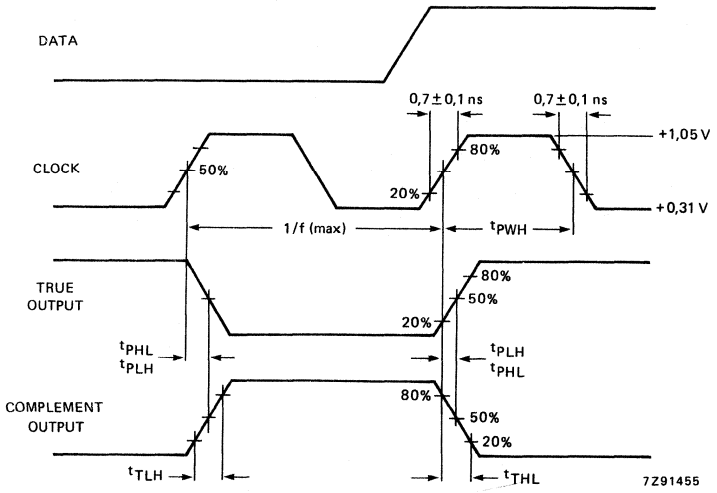


Fig. 5 Propagation delay (Clock) and transition times.

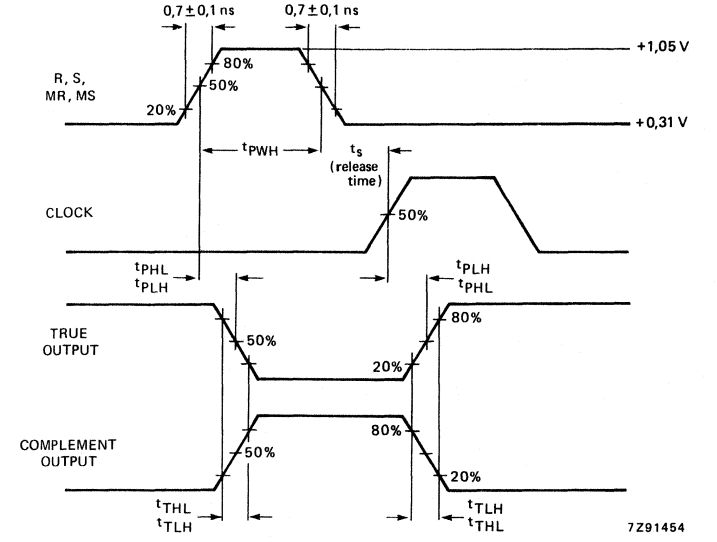


Fig. 6 Propagation delay (Resets).

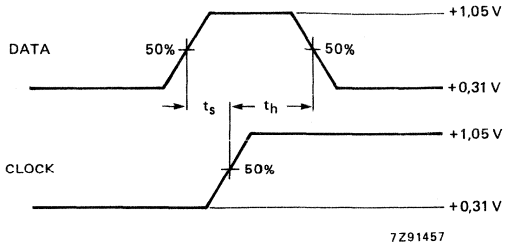


Fig. 7 Data set-up and hold time.

Notes: t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

TRIPLE D-TYPE MASTER-SLAVE FLIP-FLOP

The device has three D-type master-slave flip-flops with direct and complement outputs, separate clock, set and reset. In addition, all three flip-flops have a common clock, set and reset.

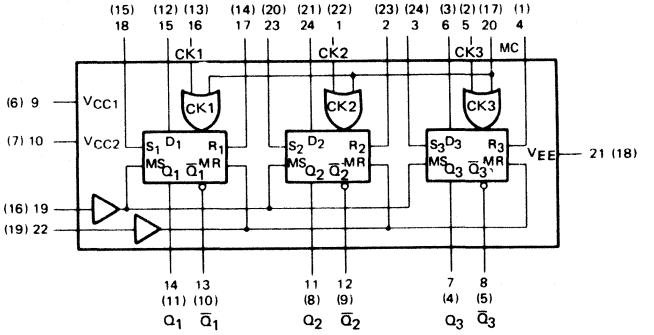


Fig. 1 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

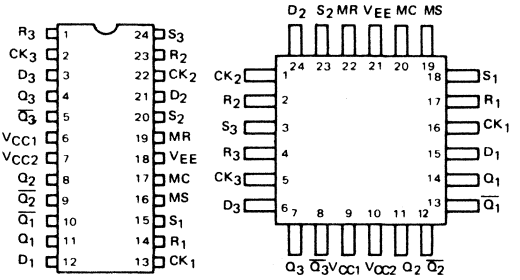


Fig. 2 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH},t_{PHL}	typ.	1.3 ns
Power consumption per package	P_{av}	typ.	495 mW

FAMILY DATA see Family Specifications
PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100131AY: 24-lead flat-pack; ceramic (SOT-138).
100131AF: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS							OUTPUTS	
D_i	MC	CK_i	MS	S_i	MR	R_i	Q_{n+1}	$\overline{Q_{n+1}}$
15(12)	20(17)	16(13)	19(16)	18(15)	22(19)	17(14)	14(11)	13(10)
24(21)	20(17)	1(22)	19(16)	23(20)	22(19)	2(23)	11(8)	12(9)
6(3)	20(17)	5(2)	19(16)	3(24)	22(19)	4(1)	7(1)	8(5)
x	x	x	L	L	H	x	L	H
x	x	x	L	L	x	H	L	H
x	x	x	H	x	L	L	H	L
x	x	x	x	H	L	L	H	L
x	x	x	H	x	H	x	*	*
x	x	x	H	x	x	H	*	*
x	x	x	x	H	H	x	*	*
x	x	x	x	H	x	H	*	*
x	x	⎍	L	L	L	L	Q_n	$\overline{Q_n}$
x	⎍	H	L	L	L	L	Q_n	$\overline{Q_n}$
x	x	x	L	L	L	L	Q_n	$\overline{Q_n}$
H	⎍	L	L	L	L	L	H	L
L	⎍	L	L	L	L	L	L	H
H	L	⎍	L	L	L	L	H	L
L	L	⎍	L	L	L	L	L	H

D_i = Data input
MS = Master Set
R_i = Reset
n = state before transition

MC = Master Clock
S_i = Set
Q = direct Output
n+1 = state after transition

CK_i = Clock
MR = Master Reset
$\overline{Q}$ = Complement Output
⎍ = LOW to HIGH transition

DATA enters a master, when both CLOCK and MASTER CLOCK are LOW, and transfers to the slave, when the CLOCK or MASTER CLOCK (or both) go HIGH. If the SET (or MASTER SET) is HIGH while the RESET (or MASTER RESET) is HIGH, the output is indefined.

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)
* = output is indefined

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
D_i, CK_i	I_{IH}	–	–	240	μA	
Mc, MS, MR	I_{IH}	–	–	450	μA	$V_{in} = V_{IHmax}$
R_i, S_i	I_{IH}	–	–	530	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	74	110	149	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; $V_{CC1} = V_{CC2}$ = ground

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
MC to OUTPUT	t_{PLH} t_{PHL}	0,75	1,80	0,75	1,80	0,75	1,85	ns	Figs 3 and 5
CK_i to output	t_{PLH} t_{PHL}	0,70	1,60	0,70	1,60	0,70	1,70	ns	
MR, MS to output									
MC, CK_i LOW	t_{PLH} t_{PHL}	1,05	2,30	1,05	2,30	1,05	2,40	ns	
MC, CK_i HIGH	t_{PLH} t_{PHL}	1,10	2,60	1,10	2,50	1,10	2,70	ns	Figs 3 and 6
R_i, S_i to output									
MC, CK_i LOW	t_{PLH} t_{PHL}	0,65	1,50	0,70	1,50	0,70	1,70	ns	
MC,CK_i HIGH	t_{PLH} t_{PHL}	0,70	1,80	0,70	1,70	0,70	2,00	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,40	0,45	1,40	ns	see Figs 3, 5 and 6
Set-up time data	t_s	0,80	–	0,60	–	0,80	–	ns	see Fig. 7
Hold time data	t_h	0,50	–	0,50	–	0,50	–	ns	see Fig. 7
Release time									
R_i and S_i	t_r	1,20	–	1,20	–	1,30	–	ns	see Fig. 6
MR and MS	t_r	2,10	–	2,10	–	2,20	–	ns	
Toggle frequency	f_{max}	400	–	400	–	400	–	MHz	see Figs 4 and 5
Pulse width HIGH									
MC,MR,MS,CK_i R_i and S_i	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Figs 5 and 6

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
MC to OUTPUT	t_{PLH} t_{PHL}	0,75	2,00	0,75	2,00	0,75	2,05	ns	Figs 3 and 5
CK_i to output	t_{PLH} t_{PHL}	0,70	1,80	0,70	1,80	0,70	1,90	ns	
MR, MS to output									
MC, CK_i LOW	t_{PLH} t_{PHL}	1,05	2,50	1,05	2,50	1,05	2,50	ns	
MC, CK_i HIGH	t_{PLH} t_{PHL}	1,10	2,80	1,10	2,70	1,10	2,90	ns	
R_i, S_i to output									Figs 3 and 6
MC, CK_i LOW	t_{PLH} t_{PHL}	0,65	1,70	0,70	1,70	0,70	1,90	ns	
MC,CK_i HIGH	t_{PLH} t_{PHL}	0,70	2,00	0,70	1,90	0,70	2,20	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,40	0,45	1,40	ns	see Figs 3, 5 and 6
Set-up time data	t_s	0,90	–	0,70	–	0,90	–	ns	see Fig. 7
Hold time data	t_h	0,60	–	0,60	–	0,70	–	ns	see Fig. 7
Release time									
R_i and S_i	t_r	1,40	–	1,30	–	1,50	–	ns	see Fig. 6
MR and MS	t_r	2.30	–	2,30	–	2,40	–	ns	
Toggle frequency	f_{max}	400	–	400	–	400	–	MHz	see Figs 4 and 5
Pulse width HIGH									
MC,MR,MS,CK_i R_i and S_i	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Figs 5 and 6

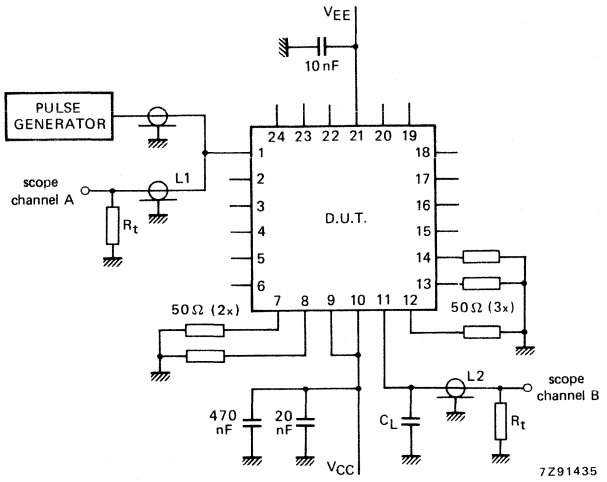


Fig. 3 Switching time test circuit.

Notes:
$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

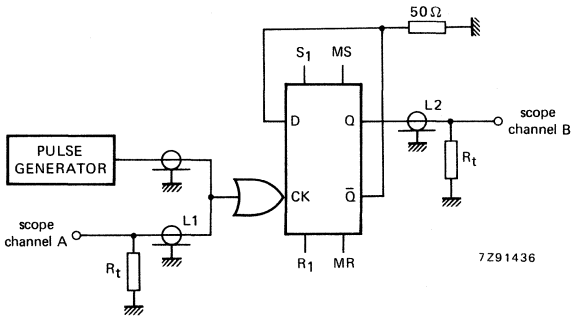


Fig. 4 Toggle frequency test circuit.

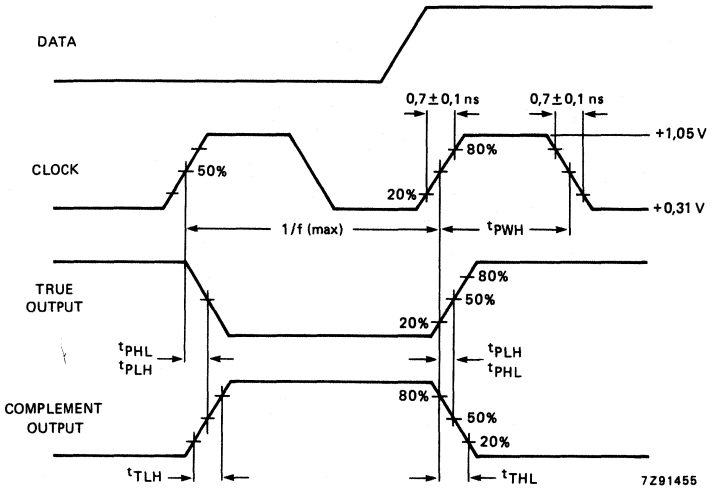


Fig. 5 Propagation delay (Clock) and transition times.

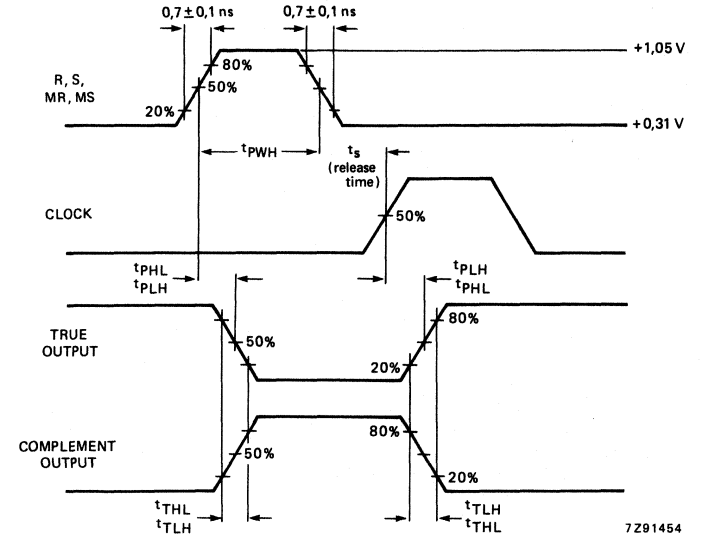


Fig. 6 Propagation delay (Resets).

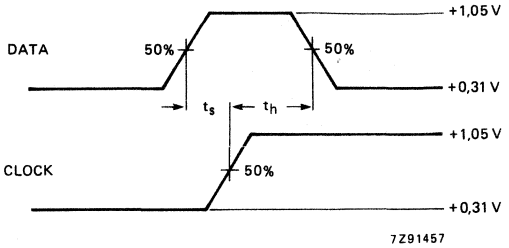


Fig. 7 Data set-up and hold time.

Notes: t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

FOUR BIT COUNTER - SHIFT REGISTER

The device operates as a 4-bit up/down counter, or as a 4-bit up/down shift register; the operating mode is determined by three selection inputs S_n. These selection inputs also permit parallel loading, synchronous reset or complement of flip-flop outputs. D_0 is the serial input for up shifting, D_3 for down shifting. In counting operations the $\overline{TC}$ output goes LOW when the counter reaches 15 in the count-up mode or 0 in the count-down mode. In the shift mode (set by $S_{0,1,2}$) $\overline{TC}$ repeats the Q_3 output. A HIGH signal at MR enables asynchronous master reset.
Two count enables ($\overline{CEP}$ and $\overline{CET}$) allow multi-stage counter cascading.

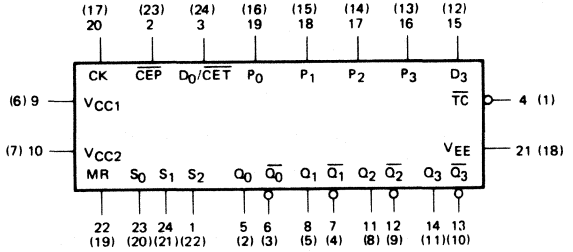


Fig. 1 Pin numbers of SLIM CERDIP package are between brackets.

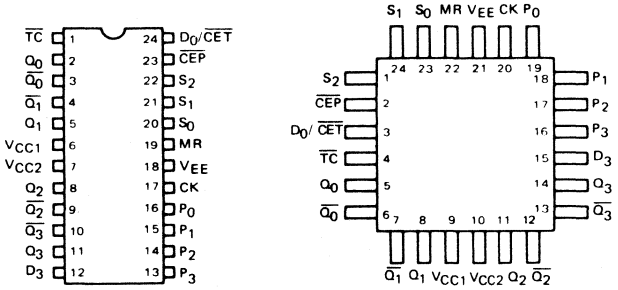


Fig. 2 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	-4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH},t_{PHL}	typ.	1,8 ns
Power consumption per package	P_{av}	typ.	945 mW

FAMILY DATA see Family Specifications
PACKAGE OUTLINES (see chapter Package Outlines)
ORDERING INFORMATION
100136Y: 24-lead flat-pack; ceramic (SOT-138).
100136F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS								OUTPUTS					mode
MR	S_0	S_1	S_2	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	
H	L	L	L	x	x	x	x	L	L	L	L	L	
H	L	H	L	x	x	x	x	L	L	L	L	L	
H	H	H	L	x	x	x	x	L	L	L	L	L	
H	L	L	H	x	L	x	x	L	L	L	L	L	
H	L	L	H	x	H	x	x	L	L	L	L	H	master reset
H	L	H	H	x	x	x	x	L	L	L	L	H	
H	H	H	H	x	x	x	x	L	L	L	L	H	
H	H	L	L	x	x	x	x	L	L	L	L	L	
H	H	L	H	x	x	x	x	L	L	L	L	H	
L	L	L	L	x	x	x	⎍	P_0	P_1	P_2	P_3	L	Preset
L	L	L	H	L	L	x	⎍	(Q_{0-3}) minus 1				1)	Count down
L	L	L	H	H	L	x	x	Q_0	Q_1	Q_2	Q_3	1)	Count down with $\overline{CEP}$ not active
L	L	L	H	x	H	x	x	Q_0	Q_1	Q_2	Q_3	H	Count down with $\overline{CET}$ not active
L	L	H	L	x	x	x	⎍	Q_1	Q_2	Q_3	D_3	D_3	Shift down
L	L	H	H	L	L	x	⎍	(Q_{0-3}) plus 1				2)	Count up
L	L	H	H	H	L	x	x	Q_0	Q_1	Q_2	Q_3	2)	Count up with $\overline{CEP}$ not active
L	L	H	H	x	H	x	x	Q_0	Q_1	Q_2	Q_3	H	Count up with $\overline{CET}$ not active
L	H	L	L	x	x	x	⎍	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	x	x	x	⎍	L	L	L	L	H	Clear
L	H	H	L	x	x	x	⎍	D_0	Q_0	Q_1	Q_2	Q_2	Shift up
L	H	H	H	x	x	x	x	Q_0	Q_1	Q_2	Q_3	H	Hold

Notes:
1) L if Q_0 to Q_3 = L L L L ; H if Q_0 to $Q_3 \neq$ L L L L
2) L if Q_0 to Q_3 = H H H H ; H if Q_0 to $Q_3 \neq$ H H H H

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)
⎍ = LOW to HIGH transition

RATINGS see Family Specifications.

SELECTION TABLE

S_0	S_1	S_2	Operating modes
L	L	L	parallel load; DATA available on P_n will be loaded with next clock pulse
L	L	H	down counter; each clock pulse deceases the counter value
L	H	L	shift down; each clock pulse shifts D_3 to Q_3, Q_n to Q_{n-1}
L	H	H	up counter; each clock pulse increases the counter value complement mode; contents of flip-flop can be synchronously inverted
H	L	L	complement mode; contents of flip-flop can be synchronously inverted
H	L	H	reset; enables a synchronous reset
H	H	L	shift up; each clock pulse shifts Q_n to Q_{n+1}, D_0 to Q_0
H	H	H	hold mode; no change for Q_n

The TC output can be connected to the $D_0/\overline{CET}$ input of another 100136 for multi-stage counting of shift up operation.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC} = V_{CC2}$ = ground, T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
P_n, S_n	I_{IH}	–	–	180	μA	
$\overline{CEP}$	I_{IH}	–	–	200	μA	
MR	I_{IH}	–	–	240	μA	$V_{in} = V_{IHmax}$
D_3	I_{IH}	–	–	280	μA	
CK	I_{IH}	–	–	390	μA	
$D_0/\overline{CET}$	I_{IH}	–	–	530	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	136	210	283	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
CK to Q_n,$\overline{Q}_n$	t_{PLH} t_{PHL}	0,85	2,35	0,85	2,35	0,85	2,50	ns	see Figs 3 and 5
CK to $\overline{TC}$	t_{PLH} t_{PHL}	1,80	5,00	1,80	4,80	1,80	5,40	ns	
MR to Q_n,$\overline{Q}_n$	t_{PLH} t_{PHL}	1,20	3,15	1,35	3,15	1,20	3,30	ns	see Figs 3 and 6
MR to $\overline{TC}$	t_{PLH} t_{PHL}	2,10	5,00	2,10	5,00	2,10	5,50	ns	
D_0/$\overline{CET}$ to $\overline{TC}$	t_{PLH} t_{PHL}	1,40	3,40	1,40	3,40	1,40	3,70	ns	see Figs 3 and 7
S_n to $\overline{TC}$	t_{PLH} t_{PHL}	1,40	5,00	1,60	5,00	1,60	5,50	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,80	0,45	1,80	0,45	1,80	ns	see Figs 3, 5, 6 and 7
Set-up time									
D_3, D_0	t_s	2,30	–	2,30	–	2,30	–	ns	see Fig. 8
P_n	t_s	2,30	–	2,30	–	2,30	–	ns	
CET, $\overline{CEP}$	t_s	2,30	–	2,30	–	2,30	–	ns	
S_n	t_s	3,80	–	3,80	–	3,80	–	ns	
Hold time									
D_3, D_0	t_h	0,40	–	0,40	–	0,40	–	ns	see Fig. 8
P_n	t_h	0,30	–	0,30	–	0,30	–	ns	
CET, $\overline{CEP}$	t_h	0,40	–	0,40	–	0,40	–	ns	
S_n	t_h	–0,2	–	–0,2	–	–0,2	–	ns	
Release time									
MR	t_r	2,80	–	2,80	–	2,80	–	ns	see Fig. 6
Shift frequency	f_{max}	250	–	250	–	250	–	MHz	see Figs 4 and 5
Pulse width HIGH									
CK, R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Figs 5 and 6

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
CK to Q_n,$\overline{Q}_n$	t_{PLH} t_{PHL}	0,85	2,15	0,85	2,15	0,85	2,30	ns	see Figs 3 and 5
CK to $\overline{TC}$	t_{PLH} t_{PHL}	1,80	4,80	1,80	4,60	1,80	5,20	ns	
MR to Q_n,$\overline{Q}_n$	t_{PLH} t_{PHL}	1,20	2,95	1,35	2,95	1,20	3,10	ns	see Figs 3 and 6
MR to $\overline{TC}$	t_{PLH} t_{PHL}	2,10	4,80	2,10	4,80	2,10	5,30	ns	
D_0/$\overline{CET}$ to $\overline{TC}$	t_{PLH} t_{PHL}	1,40	3,20	1,40	3,20	1,40	3,50	ns	see Figs 3 and 7
S_n to $\overline{TC}$	t_{PLH} t_{PHL}	1,40	4,80	1,60	4,80	1,60	5,30	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,80	0,45	1,80	0,45	1,80	ns	see Figs 3, 5, 6 and 7
Set-up time									
D_3, D_0	t_s	2,10	–	2,10	–	2,10	–	ns	
P_n	t_s	2,10	–	2,10	–	2,10	–	ns	see Fig. 8
CET, $\overline{CEP}$	t_s	2,10	–	2,10	–	2,10	–	ns	
S_n	t_s	3,60	–	3,60	–	3,60	–	ns	
Hold time									
D_3, D_0	t_h	0,20	–	0,20	–	0,20	–	ns	
P_n	t_h	0,10	–	0,10	–	0,10	–	ns	see Fig. 8
CET, $\overline{CEP}$	t_h	0,20	–	0,20	–	0,20	–	ns	
S_n	t_h	–0,4	–	–0,4	–	–0,4	–	ns	
Release time									
MR	t_r	2,60	–	2,60	–	2,60	–	ns	see Fig. 6
Shift frequency	f_{max}	250	–	250	–	250	–	MHz	see Figs 4 and 5
Pulse width HIGH									
CK, R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Figs 5 and 6

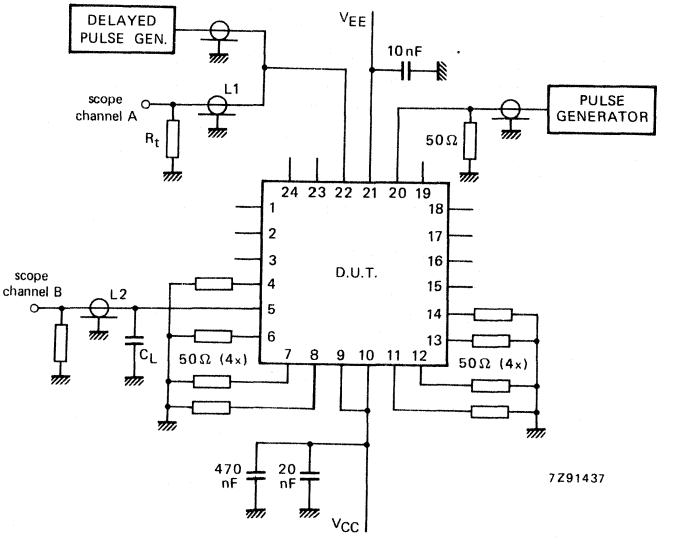


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

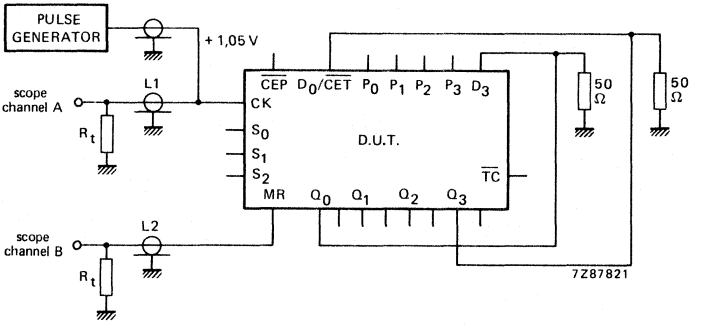


Fig. 4 Shift frequency test circuit (shift up)
$S_{0,1,2} = +1{,}05$ V.

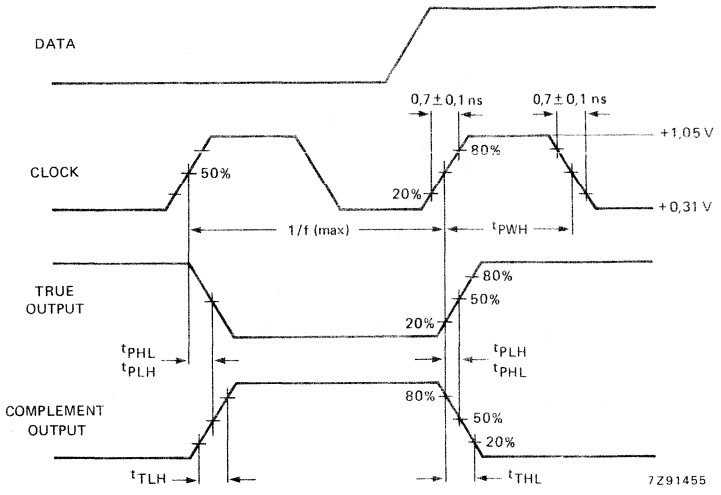


Fig. 5 Propagation delay (Clock) and transition times.

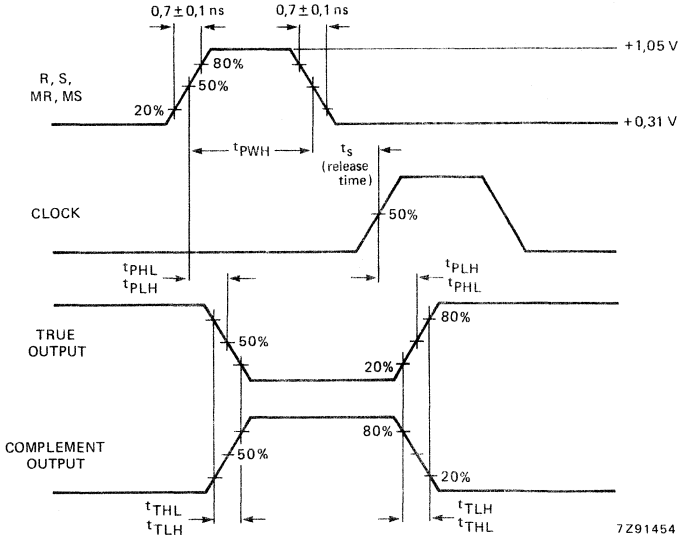


Fig. 6 Propagation delay (Reset)

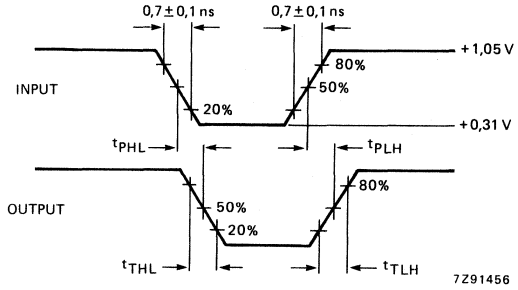


Fig. 7 Propagation delay (Serial Data, Selects)

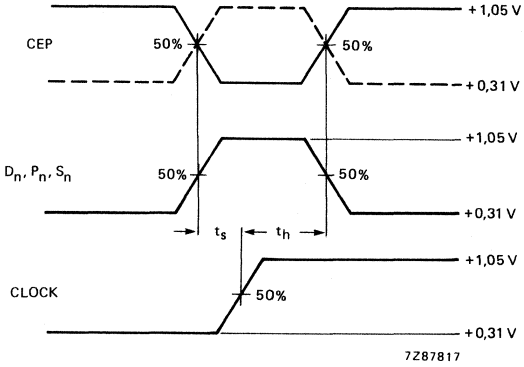


Fig. 8 Set-up and hold times.

Notes: t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

EIGHT-BIT SHIFT REGISTER

The device has eight D-type flip-flops and two selection inputs S_0 and S_1. These permit a parallel loading, left shifting, right shifting or hold operation mode.

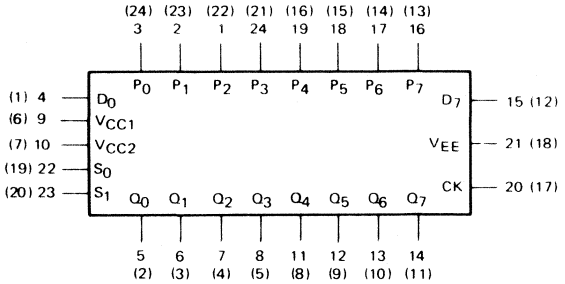


Fig. 1 Pin numbers of SLIM CERDIP package are between brackets.

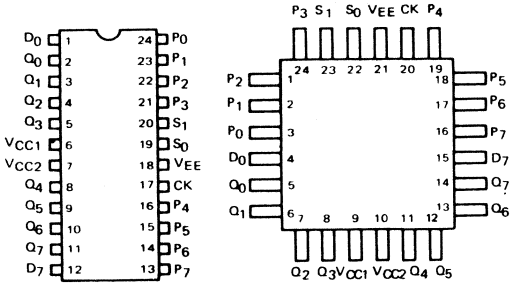


Fig. 2 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH},t_{PHL}	typ.	1,7 ns
Power consumption per package	P_{av}	typ.	785 mW

FAMILY DATA see Family Specifications
PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100141Y: 24-lead flat-pack; ceramic (SOT-138).
100141F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS			OUTPUTS								mode
S_0	S_1	CK	Q_{n+1} 7	Q_{n+1} 6	Q_{n+1} 5	Q_{n+1} 4	Q_{n+1} 3	Q_{n+1} 2	Q_{n+1} 1	Q_{n+1} 0	
L	L	⎍	7 P_n	6 P_n	5 P_n	4 P_n	3 P_n	2 P_n	1 P_n	1 P_n	register load
L	H	⎍	7 D_n	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	right shift
H	L	⎍	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	0 Q_n	0 D_n	left shift
H	H	x	7 Q_n	6 Q_n	5 Q_n	4 Q_n	3 Q_n	2 Q_n	1 Q_n	0 Q_n	hold state

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)
⎍ = LOW to HIGH transition
n = last state
n+1 = next state after transition

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
CK_n, S_n	I_{IH}	–	–	640	μA	$V_{in} = V_{IHmax}$
D_n, P_n, S_n	I_{IH}	–	–	220	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	119	175	238	mA	inputs open

RATINGS see Family Specifications.

A.C. CHARACTERISTICS

$-V_{EE}$ = 4,2 to 4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay CK to output	t_{PLH} t_{PHL}	0,90	2,40	1,10	2,40	1,10	2,55	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,30	0,45	1,40	ns	
Set-up time									
D_n, P_n	t_s	1,40	–	1,40	–	1,70	–	ns	
S_n	t_s	3,00	–	3,00	–	3,40	–	ns	see Fig. 6
Hold time									
D_n, P_n	t_h	0,60	–	0,60	–	0,60	–	ns	
S_n	t_h	0,10	–	0,10	–	0,10	–	ns	
Shift frequency	f_{max}	275	–	275	–	275	–	MHz	see Figs 4 and 5
Pulse width HIGH CK	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay CK to output	t_{PLH} t_{PHL}	0,90	2,20	1,10	2,20	1,10	2,35	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,30	0,45	1,40	ns	
Set-up time									
D_n, P_n	t_s	1,20	–	1,20	–	1,50	–	ns	
S_n	t_s	2,80	–	2,80	–	3,20	–	ns	see Fig. 6
Hold time									
D_n, P_n	t_h	0,50	–	0,50	–	0,50	–	ns	
S_n	t_h	0	–	0	–	0	–	ns	
Shift frequency	f_{max}	300	–	300	–	300	–	MHz	see Figs 4 and 5
Pulse width HIGH CK	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5

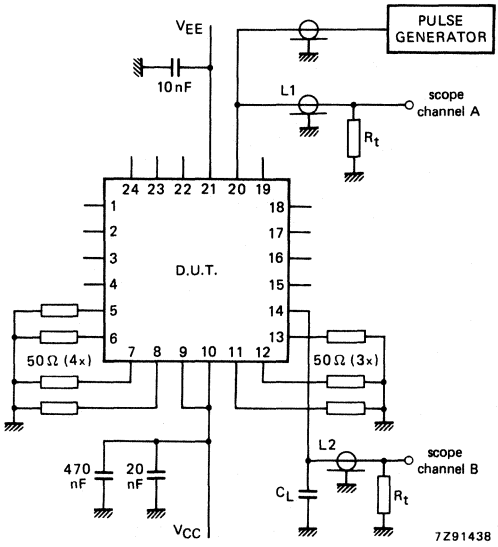


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

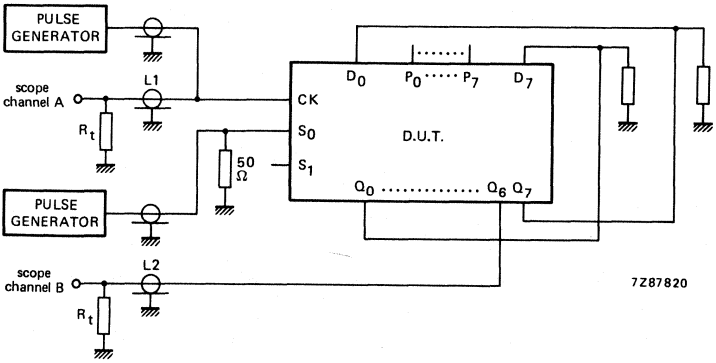


Fig. 4 Shift frequency test circuit (shift left)
P_0 to P_7 = + 1,05 V.

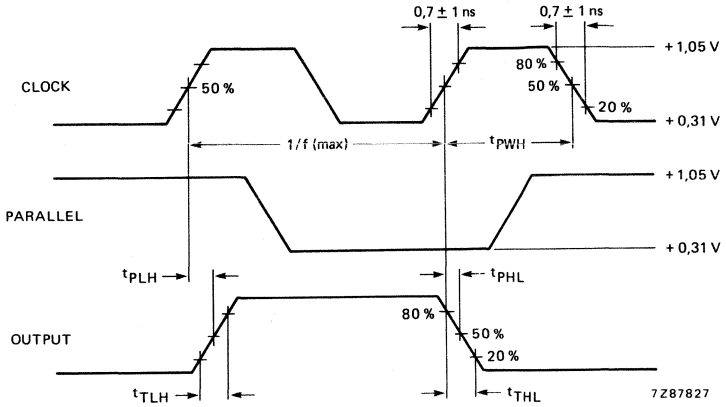


Fig. 5 Propagation delay and transition times.

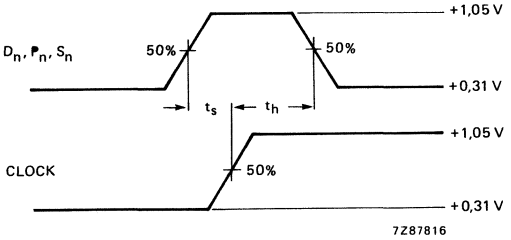


Fig. 6 Set-up and hold times.

Notes: t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

4x4 CONTENT ADDRESSABLE MEMORY

The device is a 4 word x 4 bit content addressable memory (CAM). Each word location is selected by one address line. The mask input of a data input blocks data storage. When the mask is HIGH the data input is simultaneously compared with each of the four memory words. If a search compare results in a match this output will go LOW. A HIGH mask on any bit forces a match of that bit.

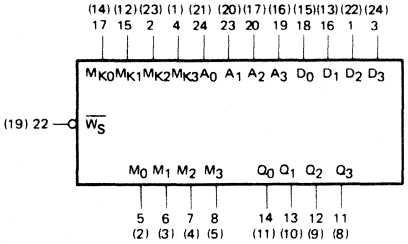


Fig. 1 Pin numbers of SLIM CERDIP package are between brackets.

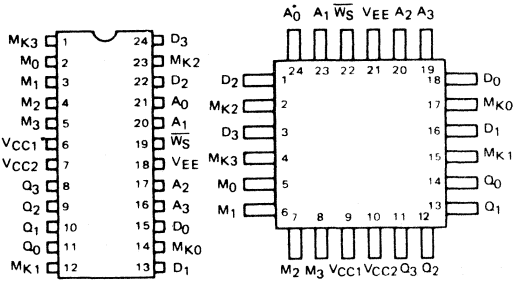


Fig. 2 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_{PLH},t_{PHL}	typ.	3,5 ns
Power consumption per package	P_{av}	typ.	855 mW

FAMILY DATA see Family Specifications
PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100142Y: 24-lead flat-pack; ceramic (SOT-138).
100142F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS				FF	OUTPUTS		mode
$\overline{WS}$	A_i	D_j	M_{Kj}	Q_{ij}	M_j	Q_j	
x	H	x	x	nc	x	L	write disabled
x	L	x	H	nc	L	Q_{ijn-1}	
H	L	x	x	nc	L	Q_{ijn-1}	
L	L	H	L	H	L	H	write
L	L	L	L	L	L	L	
H	L	x	x	H	x	H	read
H	L	x	x	L	x	L	
H	x	x	H	nc	L	x	match masked
H	L	H	L	L	H	L	match not satisfied
H	H	H	L	L	H	L	
H	H	L	L	H	H	L	
H	L	L	L	H	H	H	
H	L	H	L	H	L	H	match satisfied
H	H	H	L	H	L	L	
H	H	L	L	L	L	L	
H	L	L	L	L	L	L	

Notes:
i = for the selected word (i-th)
j = for the selected bit (j-th)
nc = no change from previous state
n-1 = previous cell state

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current						
HIGH	I_{IH}	–	–	200	μA	$V_{in} = V_{IHmax}$
LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	114	190	288	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to 4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n to Q_n	t_{AD}	1,20	4,40	1,20	4,30	1,20	4,50	ns	see Figs 3, 4, 5 and 6
D_n to M_n	t_{DM}	1,60	3,70	1,60	3,60	1,60	3,80	ns	see Figs 4, 5 and 7
MK_n to M_n	t_{MM}	1,20	3,90	1,20	3,90	1,20	4,00	ns	
Data in to data out									
D_n to Q_n	t_{DD}	1,70	4,40	1,70	4,40	1,70	4,60	ns	
Write to Data out									
$\overline{WS}$ to Q_n	t_{WD}	2,50	5,40	2,50	5,20	2,30	5,10	ns	
Address to Match									
A_n to M_n	t_{AM}	2,50	4,60	2,50	4,60	2,50	4,90	ns	see Figs 4, 5, 6
Mask to Data out									
MK_n to Q_n	t_{MD}	2,20	4,90	2,20	4,80	2,20	5,00	ns	
Write to Match									
$\overline{WS}$ to M_n	t_{WSM}	2,80	4,90	2,80	4,80	2,80	5,10	ns	
Write									
pulse width	t_w	1,40	–	1,40	–	1,40	–	ns	
Set-up time									
A to WS	t_{AS}	1,50	–	1,50	–	1,50	–	ns	
D to WS	t_{DS}	0,70	–	0,70	–	0,70	–	ns	see Fig. 6
M to WS	t_{MS}	1,20	–	1,20	–	1,20	–	ns	
Hold time									
WS to A	t_{AH}	1,50	–	1,50	–	1,50	–	ns	
WS to D	t_{DH}	1,20	–	1,20	–	1,20	–	ns	see Fig. 6
WS to M	t_{MH}	2,60	–	2,60	–	2,60	–	ns	
Transition time	t_{TLH} t_{THL}	0,50	2,20	0,50	2,20	0,50	2,20	ns	See Figs 4 and 5

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n to Q_n	t_{AD}	1,20	4,20	1,20	4,10	1,20	4,30	ns	see Figs 3, 4, 5, 6
D_n to M_n	t_{DM}	1,60	3,50	1,60	3,40	1,60	3,60	ns	
MK_n to M_n	t_{MM}	1,20	3,70	1,20	3,70	1,20	3,80	ns	see Figs 4, 5, 7
Data in to data out									
D_n to Q_n	t_{DD}	1,70	4,20	1,70	4,20	1,70	4,40	ns	
Write to Data out									
W_S to Q_n	t_{WD}	2,50	5,20	2,50	5,00	2,30	4,90	ns	
Address to Match									
A_n to M_n	t_{AM}	2,50	4,40	2,50	4,40	2,50	4,70	ns	see Figs 4, 5 and 6
Mask to Data out									
MK_n to Q_n	t_{MD}	2,20	4,70	2,20	4,60	2,20	4,80	ns	
Write to Match									
WS to M_n	t_{WSM}	2,80	4,70	2,80	4,60	2,80	4,90	ns	
Write									
pulse width	t_w	1,20	–	1,20	–	1,20	–	ns	
Set-up time									
A to WS	t_{AS}	1,30	–	1,30	–	1,30	–	ns	
D to WS	t_{DS}	0,50	–	0,50	–	0,50	–	ns	see Fig. 6
M to WS	t_{MS}	1,00	–	1,00	–	1,00	–	ns	
Hold time									
WS to A	t_{AH}	1,30	–	1,30	–	1,30	–	ns	
WS to D	t_{DH}	1,00	–	1,00	–	1,00	–	ns	see Fig. 6
WS to M	t_{MH}	2,40	–	2,40	–	2,40	–	ns	
Transition time	t_{TLH} t_{THL}	0,50	2,20	0,50	2,20	0,50	2,20	ns	See Figs 4 and 5

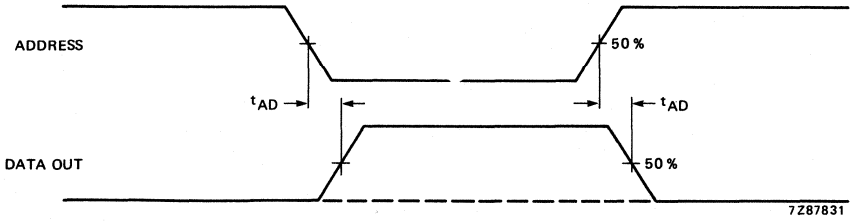


Fig. 3 Read mode waveforms.

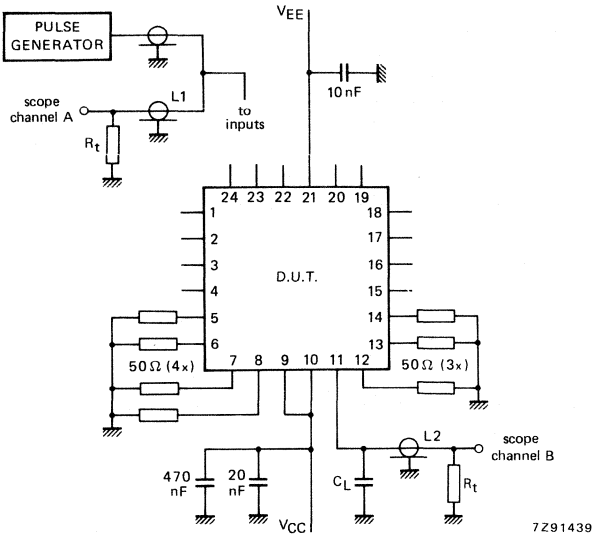


Fig. 4 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

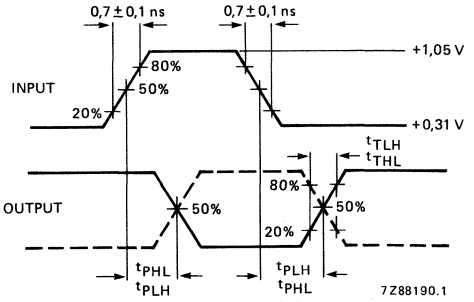


Fig. 5 Output rise and fall times.

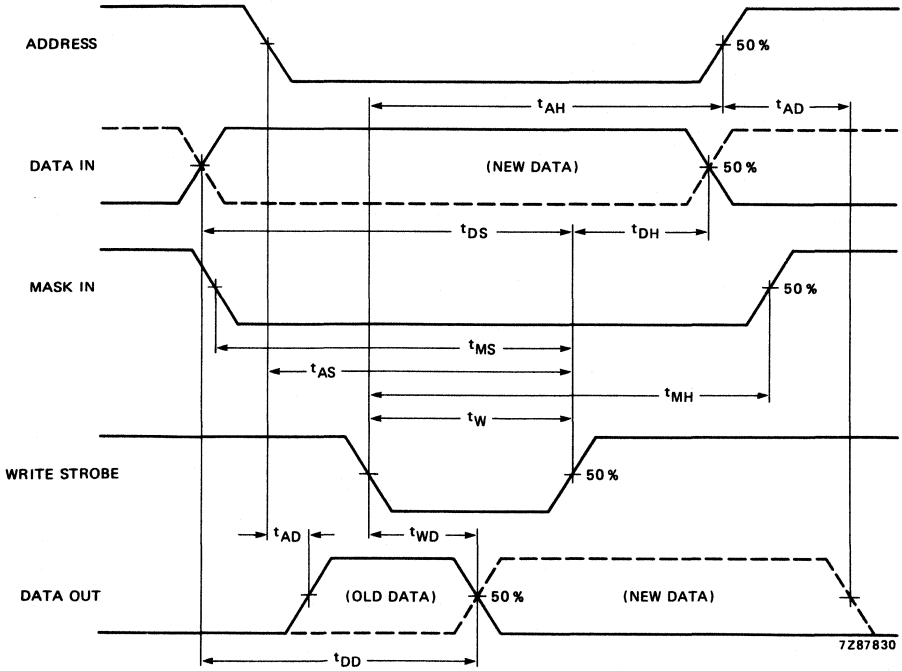


Fig. 6 Write mode and Read/Write mode waveforms.

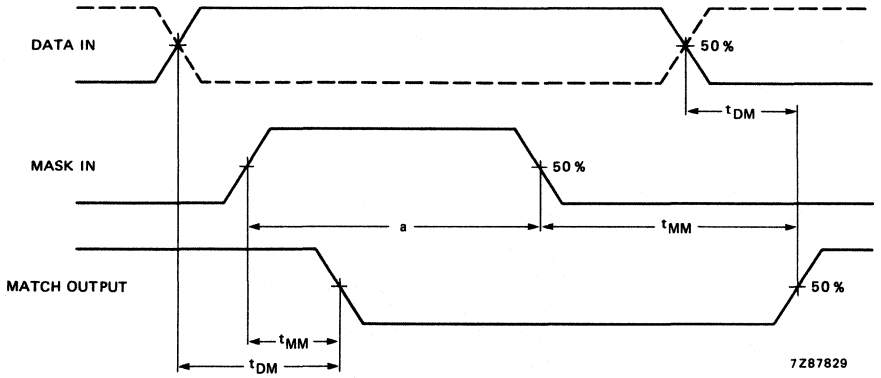


Fig. 7 Search mode waveform.
a = Mask out bit compare for one or more bits.

16x4 READ WHILE WRITE REGISTER FILE

The 100145 is a 64 bit register file organized as an array of 16 x 4. Separate address inputs for read (AR) and write (AW) are intended for shorter overall cycle time by allowing one address to be setting up, while the other is being executed. Four output latches, which store data from previous operation while writing is in progress also increase operating speed. The write enable input selects the read or write mode. In the read mode the outputs can be forced LOW by a HIGH signal on either of the output enable. One write enable input and output enable can be connected to serve as a chip select. When $\overline{CS}$ input is HIGH (with LOW other $\overline{OE}$) the circuit is in the read mode and the data are latched in the output latches and become available as soon as $\overline{CS}$ goes LOW. The master reset signal clears all cells, forces the outputs LOW and resets the output latches.

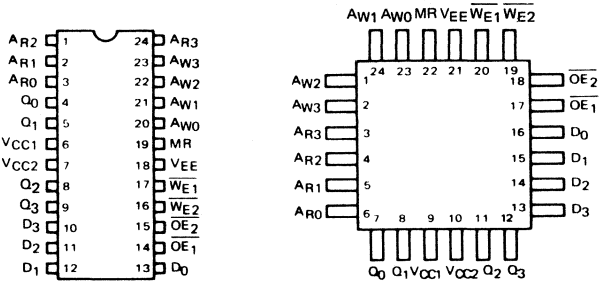


Fig. 1 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (Access time)	t_{PLH},t_{PHL}	typ.	3,5 ns
Power consumption per package	P_{av}	typ.	750 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100145Y: 24-lead flat-pack; ceramic (SOT-138)
100145F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

FUNCTION TABLE

inputs						outputs	mode	
DATA	$\overline{WE}_1$	$\overline{WE}_2$	$\overline{OE}_1$	$\overline{OE}_2$	MR	Q		
	L	L	L	L	L	data from latches	write	hold (previous operation)
	H	x	L	L	L	read data	read	data are latched
	H	x	x	H	L	L	read	data are latched
	H	x	H	x	L	L	read	data are latched
	x	H	L	L	L	read data	read	data are latched
	x	H	x	H	L	L	read	data are latched
	x	H	H	x	L	L	read	data are latched
	x	x	x	x	H	L	—	clears all cells

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial

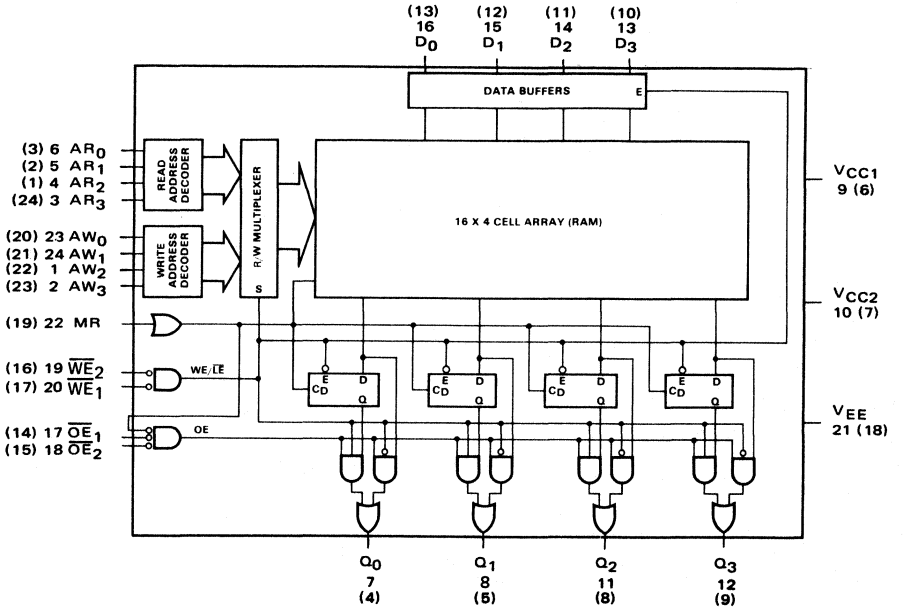


Fig. 2 Logic diagram.
Pin numbers of SLIM CERDIP package are between brackets.

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; unless otherwise specified; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current						
HIGH	I_{IH}	–	–	240	μA	$V_{in} = V_{IHmax}$
LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	119	167	247	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground

DEVELOPMENT SAMPLE DATA

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Access/Recovery									
Address access	t_{AA}	2,00	6,70	2,00	6,70	2,00	6,70	ns	see Fig. 5
Output recovery	t_{QR}	1,00	3,10	1,00	3,10	1,00	3,10	ns	see Fig. 6
Output disable	t_{QD}	1,00	3,10	1,00	3,10	1,00	3,10	ns	
Read									
Address set-up	t_{RSA1}	3,20	–	3,20	–	3,20	–	ns	see Fig. 7
Output delay	t_{WEQ}	2,00	6,10	2,00	6,10	2,00	6,10	ns	
Output latch									
Address set-up	t_{RSA2}	8,50	–	8,50	–	8,50	–	ns	see Fig. 8
Address hold	t_{RHA}	0,20	–	0,20	–	0,20	–	ns	see Fig. 9
Write									
Address set-up	t_{WSA}	3,20	–	3,20	–	3,20	–	ns	
Address hold	t_{WHA}	0,20	–	0,20	–	0,20	–	ns	
Data set-up	t_{WSD}	6,20	–	6,20	–	6,20	–	ns	see Fig. 10
Data hold	t_{MWS}	0,20	–	0,20	–	0,20	–	ns	
Pulse width	t_W	5,20	–	5,20	–	5,20	–	ns	
Master reset									
Pulse width hold	t_M	13,7	–	13,7	–	13,7	–	ns	see Fig. 11
MR to WE disable	t_{MHW}	18,4	–	18,4	–	18,4	–	ns	
MR to Q_n	t_{MQ}	3,70	–	3,70	–	3,70	–	ns	see Fig. 12
Transition time	t_{TLH} t_{THL}	0,50	2,30	0,50	2,30	0,50	2,30	ns	see Figs 3, 4

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Access/Recovery									
Address access	t_{AA}	2,00	6,50	2,00	6,50	2,00	6,50	ns	see Fig. 5
Output recovery	t_{QR}	1,00	2,90	1,00	2,90	1,00	2,90	ns	see Fig. 6
Output disable	t_{QD}	1,00	2,90	1,00	2,90	1,00	2,90	ns	
Read									
Address set-up	t_{RSA1}	3,00	–	3,00	–	3,00	–	ns	see Fig. 7
Output delay	t_{WEQ}	2,00	5,90	2,00	5,90	2,00	5,90	ns	
Output latch									
Address set-up	t_{RSA2}	8,30	–	8,30	–	8,30	–	ns	see Fig. 8
Address hold	t_{RHA}	0,00	–	0,00	–	0,00	–	ns	see Fig. 9
Write									
Address set-up	t_{WSA}	3,00	–	3,00	–	3,00	–	ns	
Address hold	t_{WHA}	0,00	–	0,00	–	0,00	–	ns	
Data set-up	t_{WSD}	6,00	–	6,00	–	6,00	–	ns	see Fig. 10
Data hold	t_{MWS}	0,00	–	0,00	–	0,00	–	ns	
Pulse width	t_W	5,00	–	5,00	–	5,00	–	ns	
Master reset									
Pulse width hold	t_M	13,5	–	13,5	–	13,5	–	ns	see Fig. 11
MR to WE disable	t_{MHW}	18,2	–	18,2	–	18,2	–	ns	
MR to Q_n	t_{MQ}	3,50	–	3,50	–	3,50	–	ns	see Fig. 12
Transition time	t_{TLH} t_{THL}	0,50	2,20	0,50	2,20	0,50	2,20	ns	see Figs 3, 4

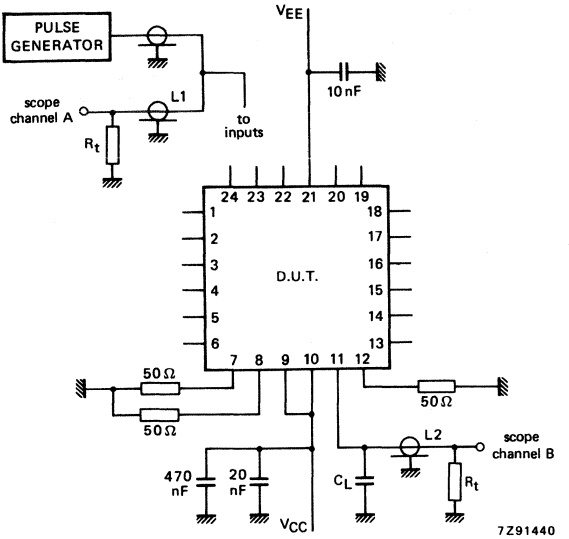


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
$R_t = 50$ Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

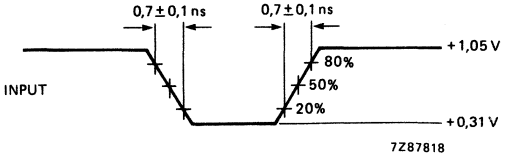


Fig. 4 Transition times.

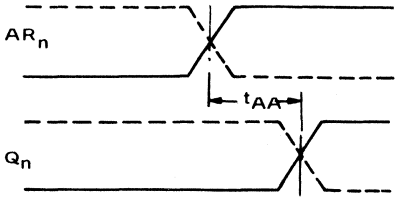


Fig. 5 Access time.
$\overline{WE}_1$ or $\overline{WE}_2$ = H; $\overline{OE}_1$ = $\overline{OE}_2$ = L

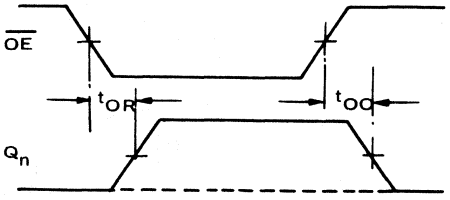


Fig. 6 Recovery time.

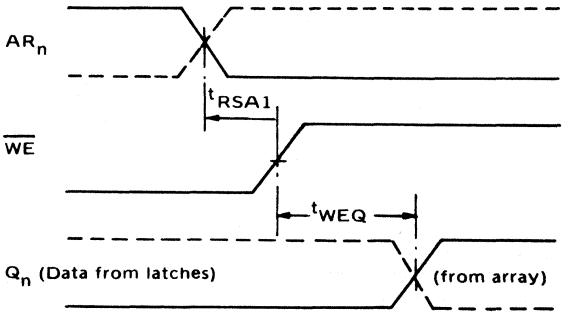


Fig. 7 Read timing

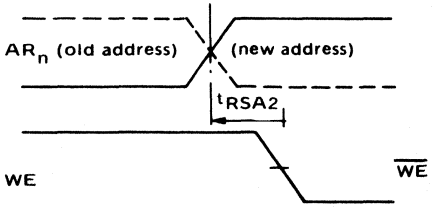


Fig. 8 Output latch timing (Set-up)

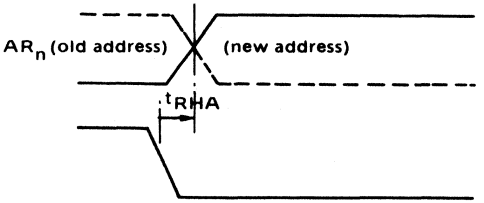


Fig. 9 Output latch timing (hold)

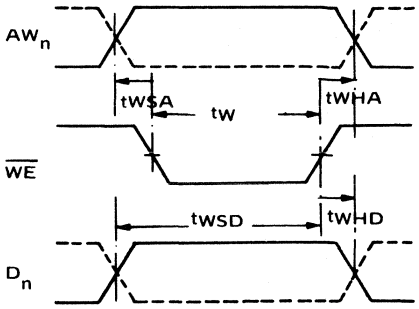


Fig. 10 Write mode set-up and hold times

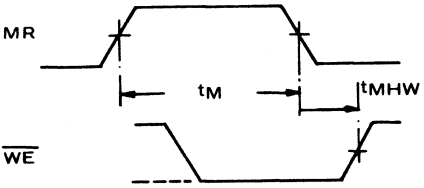


Fig. 11 Master reset pulse width and hold time.

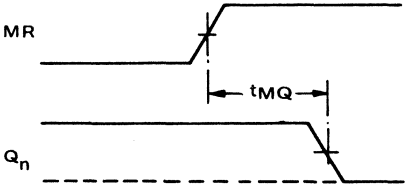


Fig. 12 Output disable time.

HEX D LATCH FLIP-FLOP

The device is composed of six latches wih data inputs, data outputs and complements. All latches have a common reset and enable. A Q-output follows its D inputs when both $\overline{E}_a$ and $\overline{E}_b$ inputs are low. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH the latches store the last valid data present on their D input. Before $\overline{E}_a$ or $\overline{E}_b$ go HIGH the R input overrides all other inputs and makes the Q-outputs LOW.

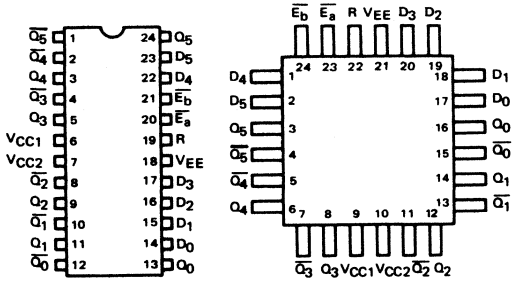


Fig. 1 Pin designation. Slim cerdip and flat pack packages

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay			
DATA	t_{PLH},t_{PHL}	typ.	0,85 ns
ENABLE	t_{PLH},t_{PHL}	typ.	1,20 ns
Power consumption per package	P_{av}	typ.	460 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100150Y: 24-lead flat-pack; ceramic (SOT-138).
100150F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS				OUTPUTS	
D	$\overline{E}_a$	$\overline{E}_b$	R	$\overline{Q}$	Q
17(14)	23(20)	24(21)	22(19)	15(12)	16(13)
18(15)	23(20)	24(21)	22(19)	13(10)	14(11)
19(16)	23(20)	24(21)	22(19)	11(8)	12(9)
20(17)	23(20)	24(21)	22(19)	7(4)	8(5)
1(22)	23(20)	24(21)	22(19)	5(2)	6(3)
2(23)	23(20)	24(21)	22(19)	4(1)	3(24)
H	L	L	L	L	H
L	L	L	L	H	L
x	x	H	L	no change	
x	H	x	L	no change	
x	x	x	H	H	L

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
R input	I_{IH}	–	–	450	μA	$V_{in} = V_{IHmax}$
D_n inputs	I_{IH}	–	–	340	μA	
$\overline{E}_a$, $\overline{E}_b$	I_{IH}	–	–	520	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	79	102	159	mA	inputs open

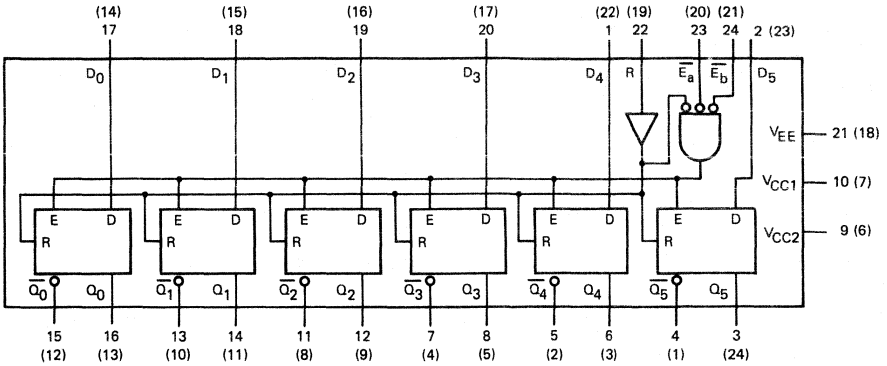


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	0,45	1,50	0,50	1,40	0,50	1,50	ns	see Figs 3 and 4
$\overline{E}$ to OUTPUT	t_{PLH} t_{PHL}	0,75	2,05	0,75	1,85	0,75	2,05	ns	
R to OUTPUT	t_{PLH} t_{PHL}	0,80	2,40	0,90	2,40	0,90	2,60	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,50	0,45	1,50	ns	see Figs 3 and 4
DATA input									
set-up time	t_s	0,70	–	0,70	–	0,70	–	ns	see Fig. 6
hold time	t_h	0,70	–	0,70	–	0,70	–	ns	
RESET input									
release time	t_r	2,10	–	2,10	–	2,10	–	ns	see Fig. 5
Pulse width									
$\overline{E}_{a,b}$ LOW	t_{PWL}	2,50	–	2,50	–	2,50	–	ns	see Fig. 4
R HIGH	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	0,45	1,30	0,50	1,20	0,50	1,30	ns	see Figs 3 and 4
$\overline{E}$ to OUTPUT	t_{PLH} t_{PHL}	0,75	1,85	0,75	1,65	0,75	1,85	ns	
R to OUTPUT	t_{PLH} t_{PHL}	0,80	2,20	0,90	2,20	0,90	2,40	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,45	1,50	0,45	1,50	0,45	1,50	ns	see Figs 3 and 4
DATA input									
set-up time	t_s	0,60	–	0,60	–	0,60	–	ns	see Fig. 6
hold time	t_h	0,60	–	0,60	–	0,60	–	ns	
RESET input									
release time	t_r	2,00	–	2,00	–	2,00	–	ns	see Fig. 5
Pulse width									
$\overline{E}_{a,b}$ LOW	t_{PWL}	2,50	–	2,50	–	2,50	–	ns	see Fig. 4
R HIGH	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5

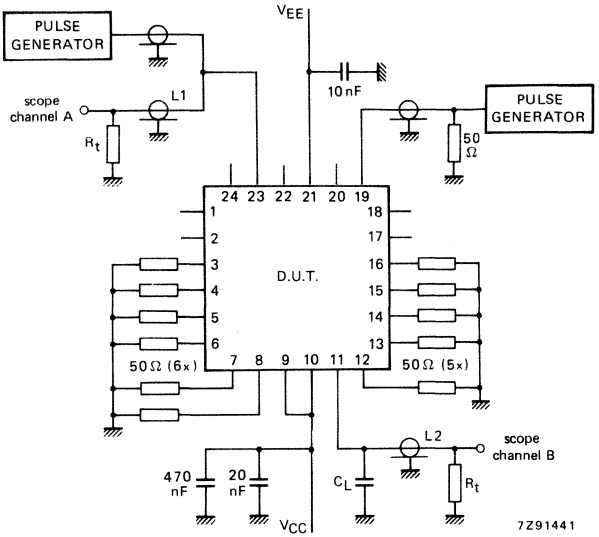


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

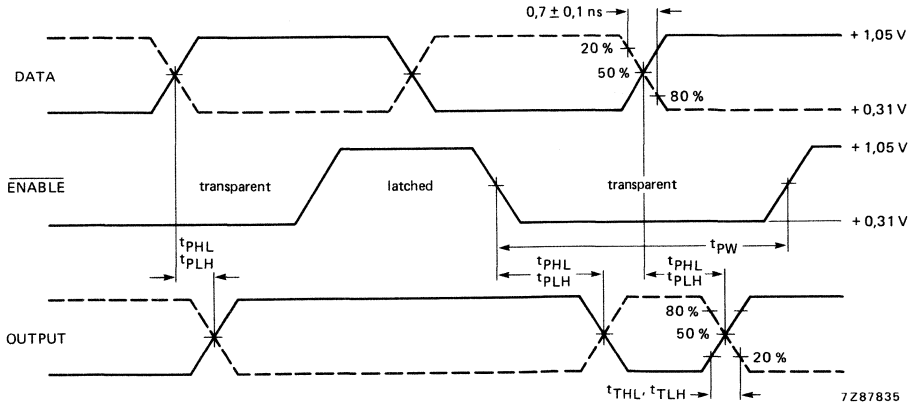


Fig. 4 Enable times waveform.

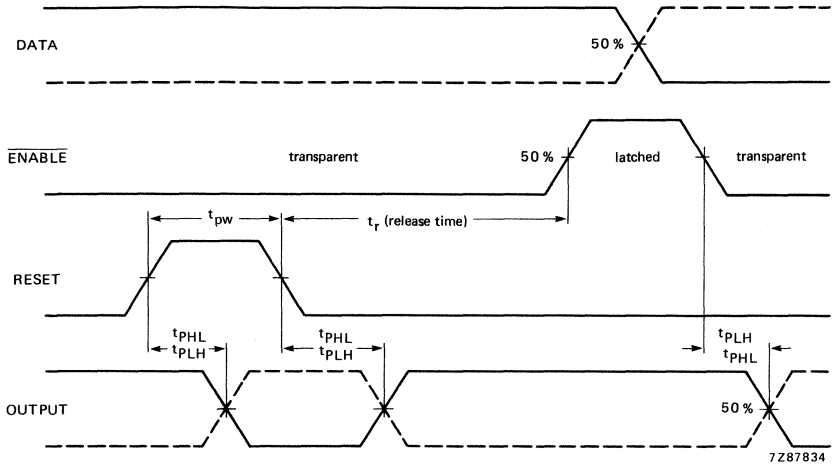


Fig. 5 Reset times waveform.

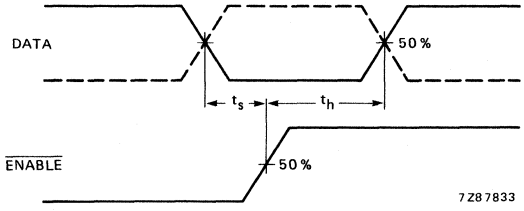


Fig. 6 DATA set-up and hold times.

Notes t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

HEX D MASTER-SLAVE FLIP-FLOP

The device contains six flip-flops with direct and complement data outputs, a common reset (R) and a pair of common clock inputs. Data enter the flip-flop on the LOW to HIGH transition of one of the two clock inputs.

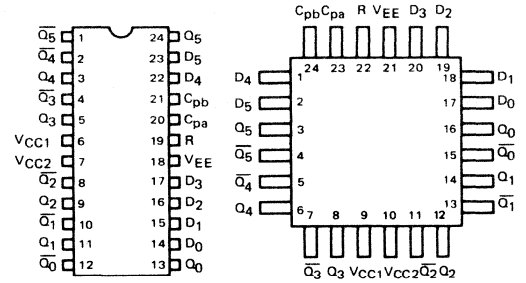


Fig. 1 Pin designation. Slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (Clock)	t_{PLH},t_{PHL}	typ.	1,7 ns
Power consumption per package	P_{av}	typ.	615 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100151Y: 24-lead flat-pack; ceramic (SOT-138).
100151F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

TRUTH TABLE

INPUTS				OUTPUTS	
D	C_{pa}	C_{pb}	R	$\overline{Q}$	Q
17(14)	23(20)	24(21)	22(19)	15(12)	16(13)
18(15)	23(20	24(21)	22(19)	13(10)	14(11)
19(16)	23(20)	24(21)	22(19)	11(8)	12(9)
20(17)	23(20)	24(21)	22(19)	7(4)	8(5)
1(22)	23(20)	24(21)	22(19)	5(2)	6(3)
2(23)	23(20)	24(21)	22(19)	4(1)	3(24)
H	L	⌐	L	L	H
L	L	⌐	L	H	L
H	⌐	L	L	L	H
L	⌐	L	L	H	L
x	x	H	L	no change	
x	H	x	L	no change	
x	x	x	H	H	L
x	L	L	L	no change	

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)
⌐ = LOW to HIGH transition

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{CC} = −4,2 to −4,8 V; unless otherwise specified;
$V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
R input	I_{IH}	–	–	450	μA	$V_{in} = V_{IHmax}$
D_n inputs	I_{IH}	–	–	225	μA	
CP_a, CP_b	I_{IH}	–	–	520	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	98	137	210	mA	Inputs open

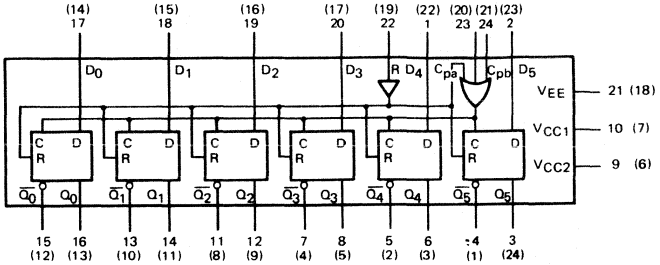


Fig. 2 Logic diagram

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
$CP_{a,b}$ to Q	t_{PLH} t_{PHL}	0,80	2,20	0,80	2,20	0,90	2,40	ns	see Figs 3 and 5
R to OTPUT	t_{PLH} t_{PHL}	1,20	2,90	1,30	3,00	1,20	3,10	ns	see Figs 3 and 6
Transition time	t_{TLH} t_{THL}	0,45	1,70	0,45	1,60	0,45	1,70	ns	see Figs 3, 5 and 6
DATA input									
set-up time	t_s	0,95	–	0,90	–	0,95	–	ns	see Fig. 7
hold time	t_h	0,70	–	0,70	–	0,70	–	ns	
RESET input release time	t_r	2,30	–	2,30	–	2,60	–	ns	Fig. 6
Pulsewidth HIGH									
$CP_{a,b}$ R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	Figs 4, 5
Toggle frequency	f_{max}	375	–	375	–	375	–	MHz	Figs 5, 6

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max		
Propagation delay									
$CP_{a,b}$ to Q	t_{PLH} t_{PHL}	0,80	2,00	0,80	2,00	0,90	2,20	ns	see Figs 3 and 5
R to OUTPUT	t_{PLH} t_{PHL}	1,20	2,70	1,30	2,80	1,20	2,90	ns	see Figs 3 and 6
Transition time	t_{TLH} t_{THL}	0,45	1,70	0,45	1,60	0,45	1,70	ns	see Figs 3, 5 and 6
DATA input									
set-up time	t_s	0,75	–	0,70	–	0,75	–	ns	see Fig. 7
hold time	t_h	0,60	–	0,60	–	0,60	–	ns	
RESET input									
release time	t_r	2,20	–	2,20	–	2,50	–	ns	Fig. 6
Pulsewidth HIGH $CP_{a,b}$ R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	Figs 4, 5
Toggle frequency	f_{max}	375	–	375	–	375	–	MHz	Figs 5, 6

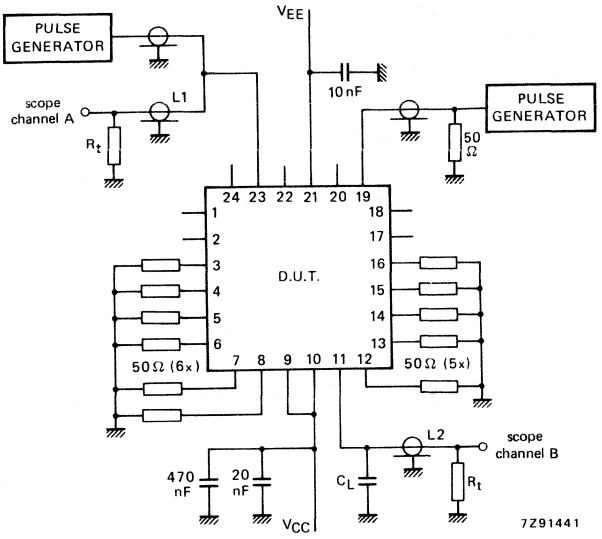


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

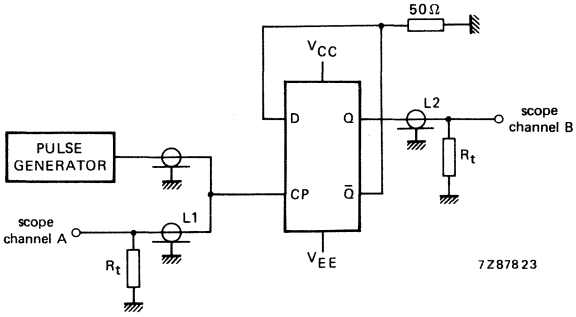


Fig. 4 Toggle frequency test circuit.

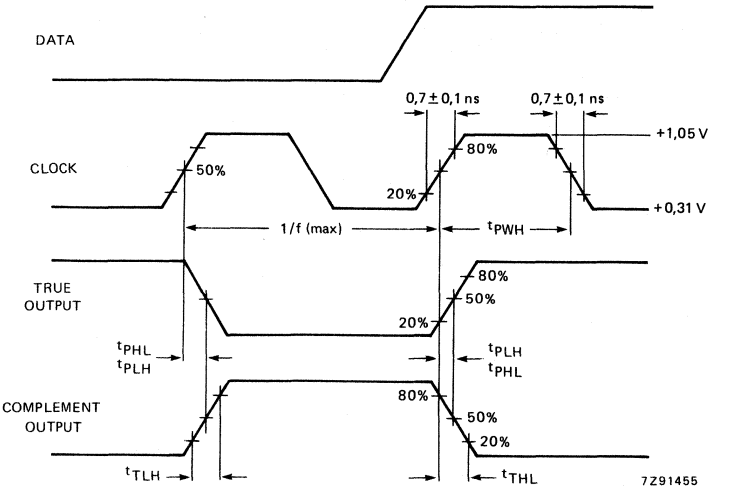


Fig. 5 Propagation delay (Clock) and transition times.

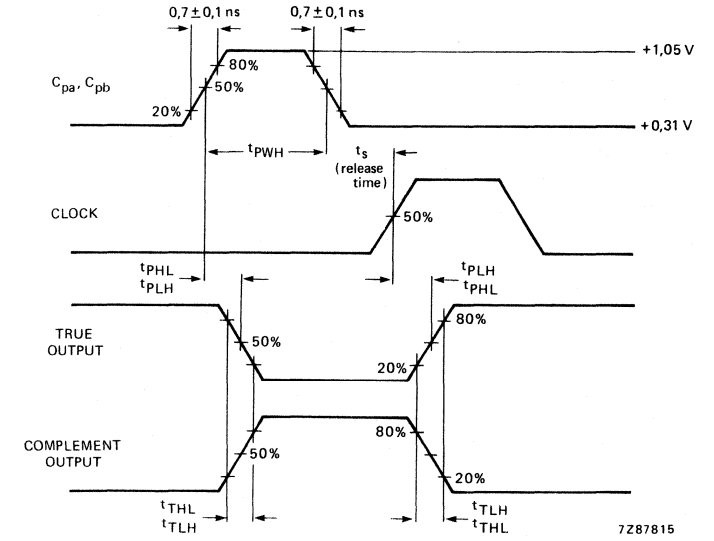


Fig. 6 Propagation delay (Reset).

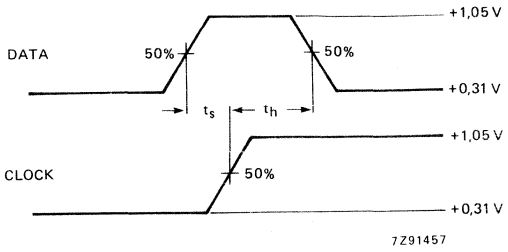


Fig. 7 Set-up and hold times.

Notes t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

QUADRUPLE 2-WAY MULTIPLEXER-LATCH

The device has four flip-flops with direct and complement data outputs, a common reset (R) and a common clock input, fed by a 2-input negative AND gate (E_1, E_2) and data inputs from a 2-way multiplexer. Each multiplexer has two data inputs selected by two common address inputs (S_0, S_1). One address input is complemented, so the address inputs can be connected together to form a single select input.

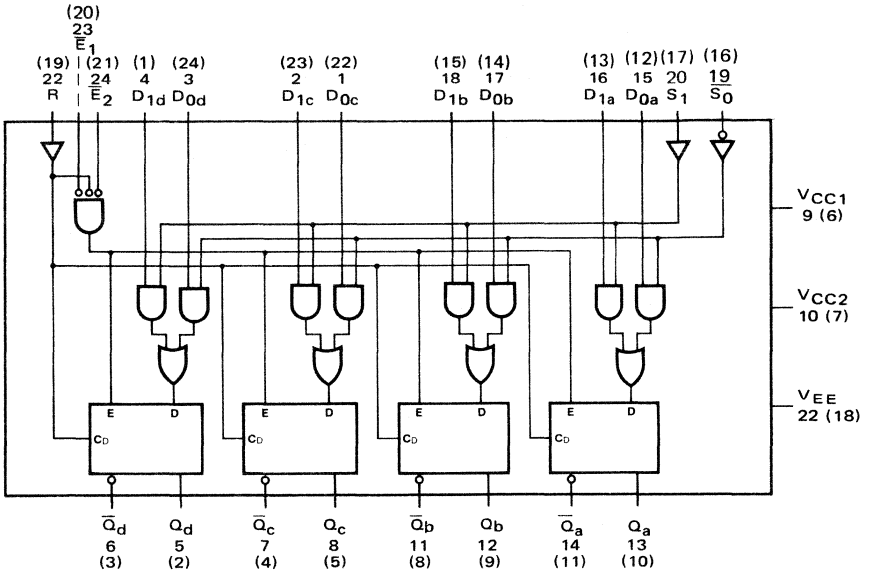


Fig. 1 Logic diagram.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (DATA)	t_{PLH},t_{PHL}	typ.	1,1 ns
Power consumption per package	P_{av}	typ.	420 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100155Y: 24-lead flat-pack; ceramic (SOT-138).
100155F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

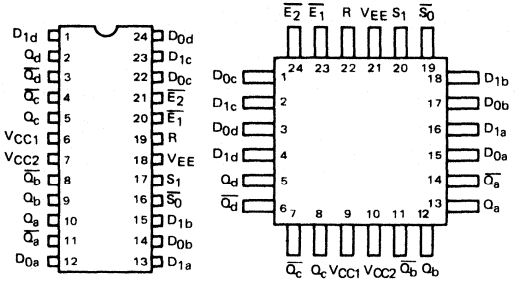


Fig. 2 Pin designation. Slim cerdip and flat pack packages.

TRUTH TABLE

INPUTS							OUTPUTS	
R	$\overline{E_1}$	$\overline{E_2}$	S_1	$\overline{S_0}$	D_1	D_0	$\overline{Q}$	Q
22(19)	23(20	24(21)	20(17)	19(16)	16(13) 18(15) 2(23) 4(1)	15(12) 17(14) 1(22) 3(24)	14(11) 11(8) 7(4) 6(3)	13(10) 12(9) 8(5) 5(2)
H	x	x	x	x	x	x	H	L
L	L	L	H	H	H	x	L	H
L	L	L	H	H	L	x	H	L
L	L	L	L	L	x	H	L	H
L	L	L	L	L	x	L	H	L
L	L	L	L	H	x	x	H	L
L	L	L	H	L	H	x	L	H
L	L	L	H	L	x	H	L	H
L	L	L	H	L	L	L	H	L
L	H	x	x	x	x	x	no change	
L	x	H	x	x	x	x	no change	

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; unless otherwise specified; V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to 85°C

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
R input	I_{IH}	–	–	430	μA	$V_{in} = V_{IHmax}$
D_n inputs	I_{IH}	–	–	340	μA	
E_n inputs	I_{IH}	–	–	350	μA	
S_n inputs	I_{IH}	–	–	220	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	66	93	133	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to Q	t_{PLH} t_{PHL}	0,50	1,90	0,60	1,85	0,50	1,90	ns	see Figs 3 and 4
S_n to output	t_{PLH} t_{PHL}	1,50	3,50	1,50	3,40	1,50	3,50	ns	see Figs 3 and 4
E_n to output	t_{PLH} t_{PHL}	0,90	2,50	1,00	2,40	1,00	2,50	ns	see Figs 3 and 4
R to output	t_{PLH} t_{PHL}	0,90	3,00	0,90	2,90	0,90	3,00	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,60	2,20	0,60	2,10	0,45	2,20	ns	see Figs 3 and 4
Set-up time									
D_n	t_s	0,90	–	0,90	–	0,90	–	ns	see Fig. 6
S_n	t_s	2,80	–	2,50	–	2,80	–	ns	see Fig. 6
Hold time									
D_n	t_h	0,50	–	0,50	–	0,50	–	ns	see Fig. 6
S_n	t_h	–0,6	–	–0,6	–	–0,6	–	ns	see Fig. 6
Release time	t_r	2,20	–	2,20	–	2,20	–	ns	see Fig. 5
Pulse width HIGH									
R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5
Pulse width LOW									
E_n	t_{PWL}	2,50	–	2,50	–	2,50	–	ns	see Fig. 4

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to Q	t_{PLH} t_{PHL}	0,50	1,70	0,60	1,65	0,50	1,70	ns	see Figs 3 and 4
S_n to output	t_{PLH} t_{PHL}	1,50	3,30	1,50	3,20	1,50	3,30	ns	see Figs 3 and 4
E_n to output	t_{PLH} t_{PHL}	0,90	2,30	1,00	2,20	1,00	2,30	ns	see Figs 3 and 4
R to output	t_{PLH} t_{PHL}	0,90	2,80	0,90	2,70	0,90	2,80	ns	see Figs 3 and 5
Transition time	t_{TLH} t_{THL}	0,60	2,20	0,60	2,10	0,45	2,20	ns	see Figs 3 and 4
Set-up time									
D_n	t_s	0,80	–	0,80	–	0,80	–	ns	see Fig. 6
S_n	t_s	2,60	–	2,30	–	2,60	–	ns	see Fig. 6
Hold time									
D_n	t_h	0,30	–	0,30	–	0,30	–	ns	see Fig. 6
S_n	t_h	–0,8	–	–0,8	–	–0,8	–	ns	see Fig. 6
Release time	t_r	2,00	–	2,00	–	2,00	–	ns	see Fig. 5
Pulse width HIGH									
R	t_{PWH}	2,50	–	2,50	–	2,50	–	ns	see Fig. 5
Pulse width LOW									
E_n	t_{PWL}	2,50	–	2,50	–	2,50	–	ns	see Fig. 4

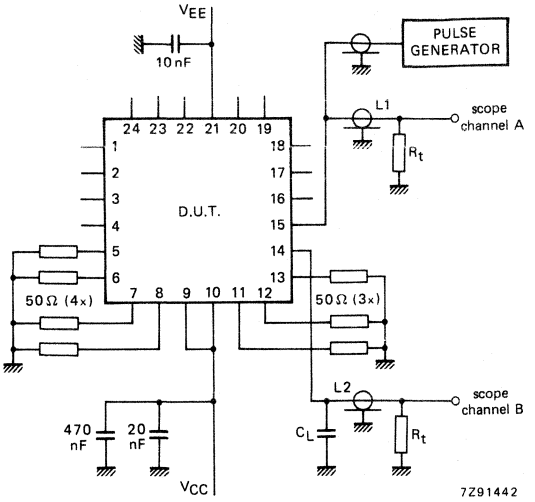


Fig. 3 Switching time test circuit.

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

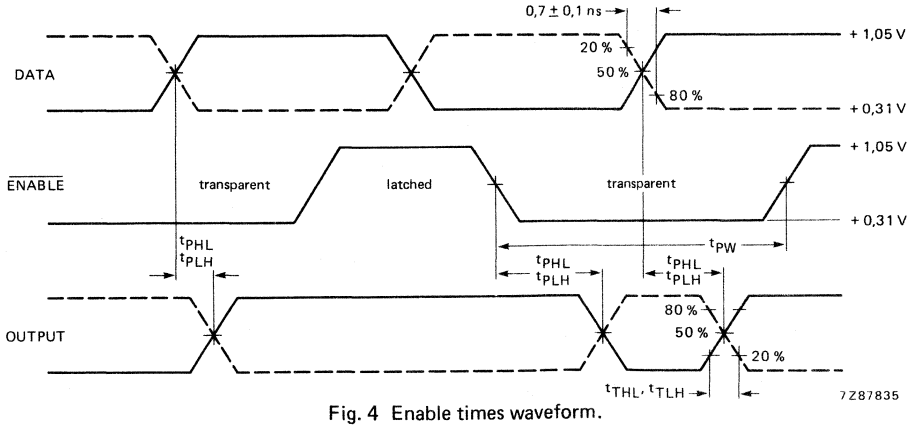


Fig. 4 Enable times waveform.

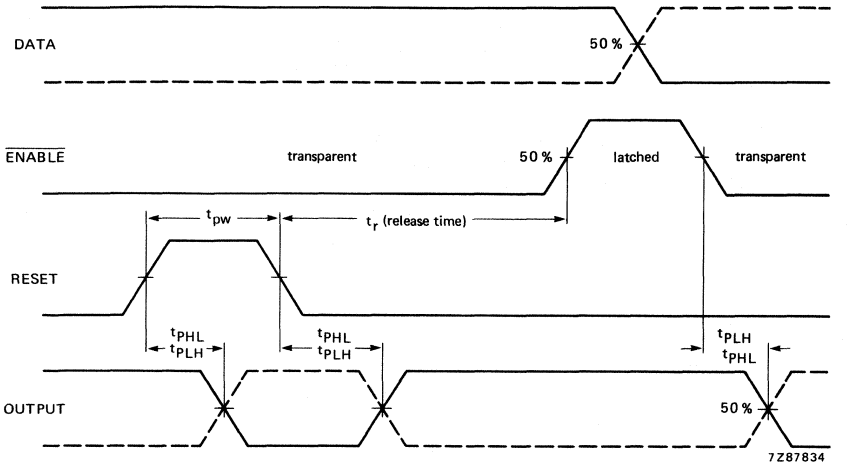


Fig. 5 Reset times waveform.

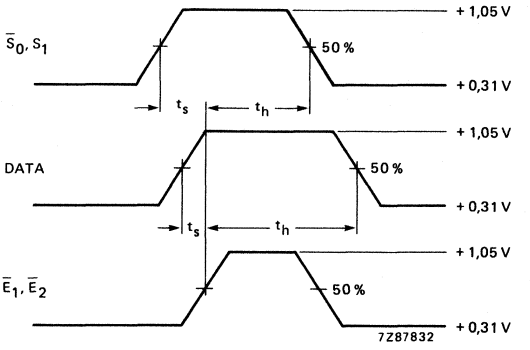


Fig. 6 Set-up and hold times waveforms.

Notes t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

8 BIT SHIFT MATRIX

The 100158 circuit shifts data bits. The three S inputs give the shift count from zero to seven. The M input forces a LOW level on the higher order bits for fill shift or enables and end around shift.

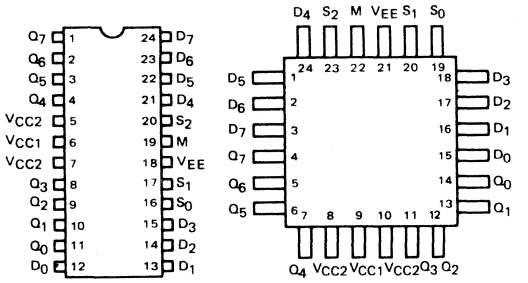


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (DATA)	t_{PLH},t_{PHL}	typ.	1,9 ns
Power consumption per package	P_D	typ.	530 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100158Y: 24-lead flat-pack; ceramic (SOT-138)
100158F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

TRUTH TABLE

INPUTS				OUTPUTS								
M	S_2	S_1	S_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	mode
22 (19)	23 (20)	20 (17)	19 (16)	4 (1)	5 (2)	6 (3)	7 (4)	11 (8)	12 (9)	13 (10)	14 (11)	
x	L	L	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	no shift
L	L	L	H	L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	left shift
L	L	H	L	L	L	D_7	D_6	D_5	D_4	D_3	D_2	
L	L	H	H	L	L	L	D_7	D_6	D_5	D_4	D_3	
L	H	L	L	L	L	L	L	D_7	D_6	D_5	D_4	
L	H	L	H	L	L	L	L	L	D_7	D_6	D_5	
L	H	H	L	L	L	L	L	L	L	D_7	D_6	
L	H	H	H	L	L	L	L	L	L	L	D_7	
H	L	L	H	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	
H	L	H	L	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	
H	L	H	H	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_4	end around carry
H	H	L	L	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
H	H	L	H	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	
H	H	H	L	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	
H	H	H	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	

Positive logic
H = 1 = HIGH state (the more positive voltage)
L = 0 = LOW state (the less positive voltage)
x = state is immaterial (H or L)

RATINGS see Family Specifications.

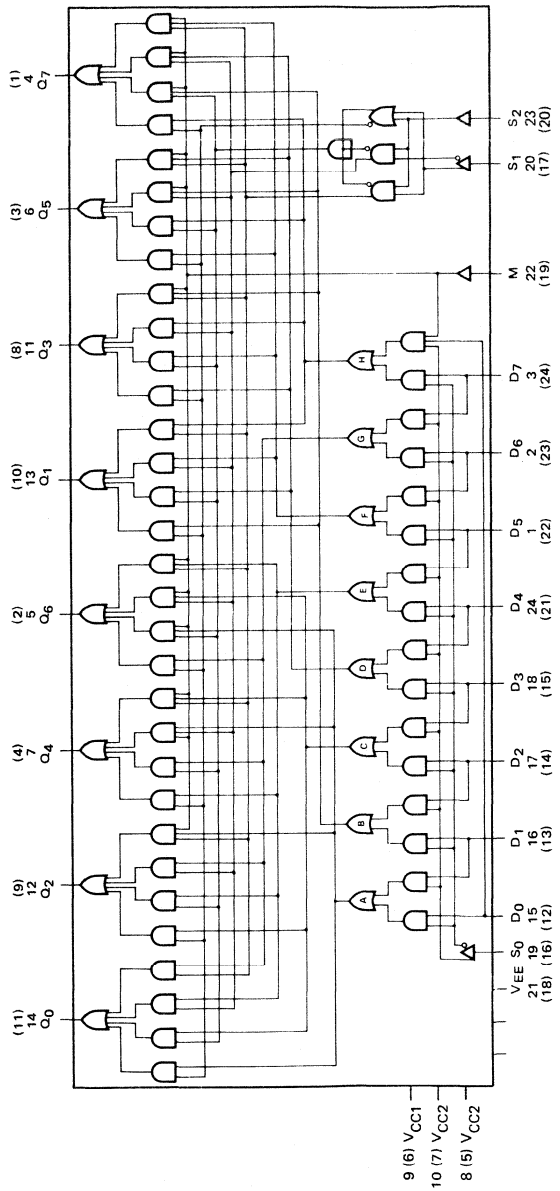


Fig. 2 Logic diagram.
Pin numbers of slim cerdip packages are between brackets.

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; unless otherwise specified; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C

description	symbol	min.	typ.	max.	unit	remarks
input current						
HIGH	I_{IH}	–	–	220	μA	$V_{in} = V_{IHmax}$
LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
supply current	$-I_{EE}$	84	118	205	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	1,10	3,00	1,10	2,90	1,10	3,10	ns	
M to output	t_{PLH} t_{PHL}	1,15	4,40	1,25	4,40	1,15	4,70	ns	
S_n to output	t_{PLH} t_{PHL}	1,70	4,50	1,70	4,50	1,70	4,80	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,50	2,20	0,50	2,20	0,50	2,20	ns	

FLATPACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	1,10	2,80	1,10	2,70	1,10	2,90	ns	
M to output	t_{PLH} t_{PHL}	1,15	4,20	1,25	4,20	1,15	4,50	ns	
S_n to output	t_{PLH} t_{PHL}	1,70	4,30	1,70	4,30	1,70	4,60	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,50	2,20	0,50	2,20	0,50	2,20	ns	

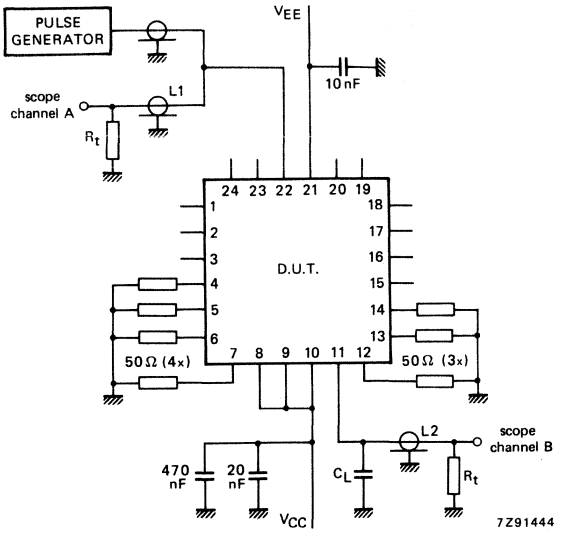


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2$ = equal length 50 Ω impedance lines.
R_t = 50 Ω terminator internal to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE}.
All unused outputs are loaded with 50 Ω to ground.
C_L = fixture and stray capacitance ⩽ 3 pF.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic symbol.

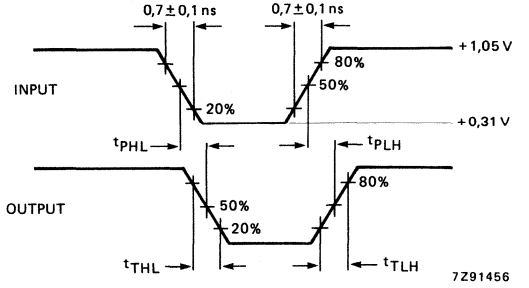


Fig. 4 Propagation delay and transition time waveforms.

DUAL 9-BIT PARITY GENERATOR/8-BIT COMPARATOR

The two parity generators each accept a 9-bit data word (D_a+D_{an}, D_b+D_{bn}) and give a parity indication at their respective outputs (Q_a, Q_b) which is HIGH when the sum of the HIGH bits of a data word is EVEN, and LOW when the sum is ODD. Expansion into other 100160 parity generators to facilitate words greater than 16 bits can be made using bits D_a, D_b as these have an extremely short propagation delay between input and output.
An 8-bit comparator is included which compares bits D_{a0} to D_{a7} with bits D_{b0} to D_{b7} and gives a LOW output ($\overline{C}$) when the two groups are equal.

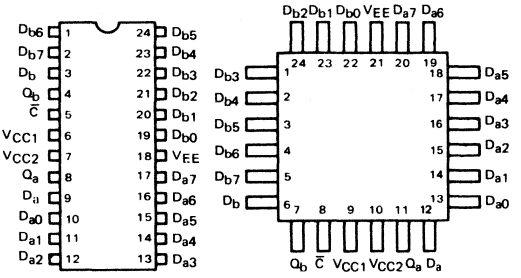


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	tp	typ.	1,8 ns
Power consumption per package	P_{av}	typ.	350 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100160Y: 24-lead flat-pack; ceramic (SOT-138)
100160F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

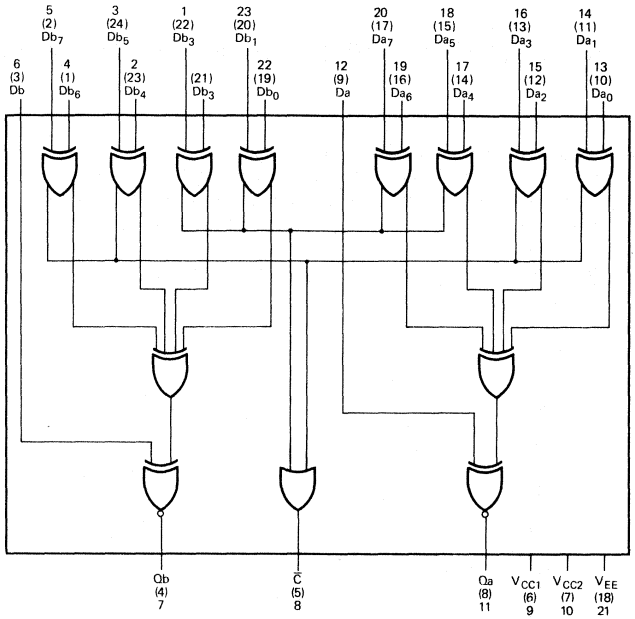


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP packages are between brackets.

TRUTH TABLE

INPUTS		OUTPUTS		
D_a, D_{a0} to D_{a7}	D_b, D_{b0} to d_{b7}	Q_a	Q_b	$\overline{C}$
sum of H bits ODD		L		
sum of H bits EVEN		H		
	sum of H bits ODD		L	
	sum of H bits EVEN		H	
$D_{a0} = D_{b0}$ and $D_{a1} = D_{b1}$ and $D_{a2} = D_{b2}$ and $D_{a3} = D_{b3}$ and $D_{a4} = D_{b4}$ and $D_{a5} = D_{b5}$ and $D_{a6} = D_{b6}$ and $D_{a7} = D_{b7}$				L
all other combinations				H

H = HIGH level L = LOW level X = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
D_a, D_b	I_{IH}	–	–	340	μA	$V_{in} = V_{IHmax}$
D_{an}, D_{bn}	I_{IH}	–	–	240	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	57	78	115	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{an},D_{bn} to Q_a,Q_b	t_{PLH} t_{PHL}	1,30	4,30	1,30	4,10	1,30	4,30	ns	
D_a,D_b to Q_a,Q_b	t_{PLH} t_{PHL}	0,50	1,60	0,50	1,60	0,50	1,60	ns	
D_{an},D_{bn} to $\overline{C}$	t_{PLH} t_{PHL}	1,20	3,30	1,20	3,10	1,20	3,30	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,40	1,70	0,40	1,65	0,40	1,65	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{an},D_{bn} to Q_a,Q_b	t_{PLH} t_{PHL}	1,30	4,10	1,30	3,90	1,30	4,10	ns	
D_a,D_b to Q_a,Q_b	t_{PLH} t_{PHL}	0,50	1,40	0,50	1,40	0,50	1,40	ns	
D_{an},D_{bn} to $\overline{C}$	t_{PLH} t_{PHL}	1,20	3,10	1,20	2,90	1,20	3,10	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,50	1,70	0,50	1,65	0,50	1,65	ns	

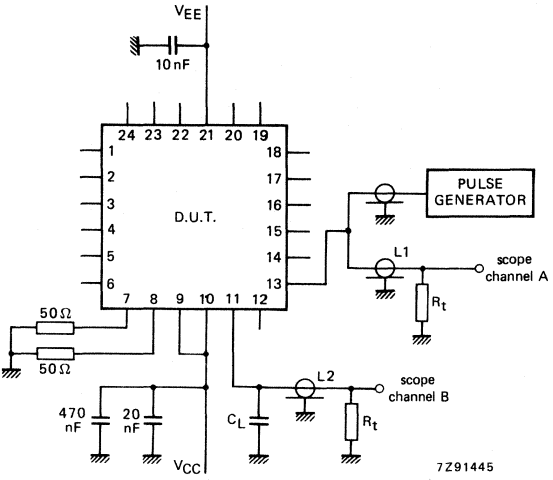


Fig. 3 A.C. test circuit.

Notes:

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -2{,}5$ V
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope;
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for flat pack, for dual in-line package see logic diagram.

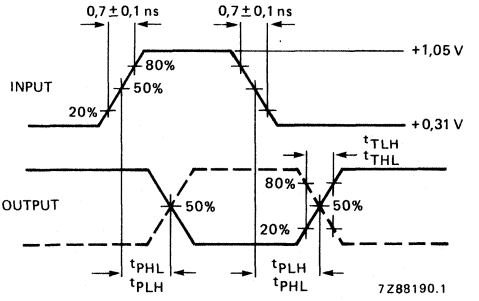


Fig. 4 Propagation delay and transition times.

DUAL 8-BIT MULTIPLEXER

The two multiplexers of the 100163 each have eight data inputs (D_{an}, D_{bn}), one data output (Q_a, Q_b) and a common, 3-bit address input (S_n). One data input per multiplexer is selected by the common address and directed to the respective outputs. Polarity of the data is not changed. Ground may be used as a substitute for HIGH levels at the address inputs.

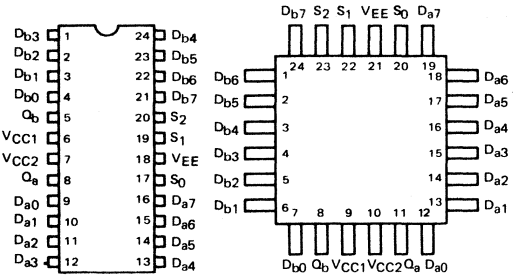


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (DATA)	tp	typ.	1,25 ns
Power consumption per package	P_{av}	typ.	560 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100163Y: 24-lead flat-pack; ceramic (SOT-138)
100163F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

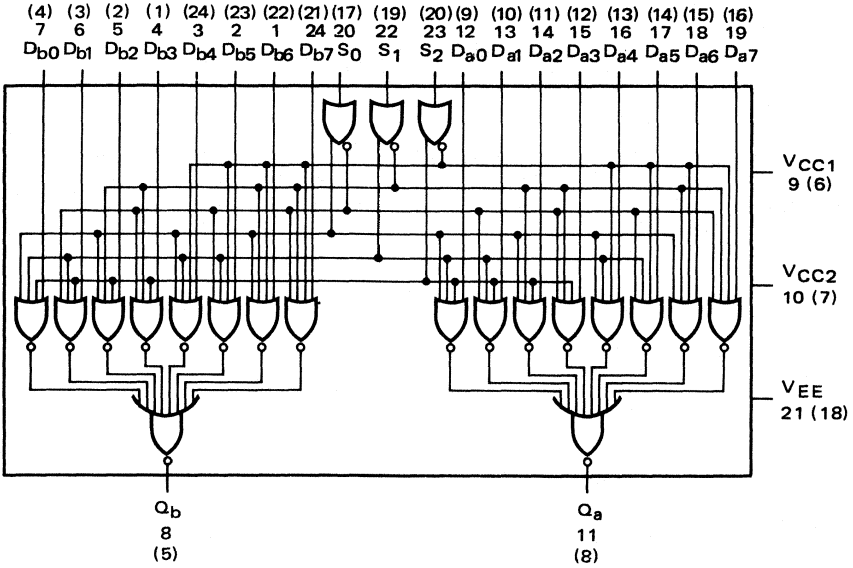


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP packages are between brackets.

TRUTH TABLE

address			data output	
S_2	S_1	S_0	Q_a	Q_b
L	L	L	D_{a0}	D_{b0}
L	L	H	D_{a1}	D_{b1}
L	H	L	D_{a2}	D_{b2}
L	H	H	D_{a3}	D_{b3}
H	L	L	D_{a4}	D_{b4}
H	L	H	D_{a5}	D_{b5}
H	H	L	D_{a6}	D_{b6}
H	H	H	D_{a7}	D_{b7}

H = HIGH level (or ground)
L = LOW level
x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
D_{an}, D_{bn}	I_{IH}	–	–	340	μA	$V_{in} = V_{IHmax}$
S_n	I_{IH}	–	–	265	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	76	125	161	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{an},D_{bn} to output	t_{PLH} t_{PHL}	0,55	1,90	0,60	1,90	0,65	2,00	ns	
S_n to output	t_{PLH} t_{PHL}	1,10	2,80	1,10	2,80	1,20	3,10	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,50	1,75	0,50	1,70	0,50	1,70	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{an},D_{bn} to output	t_{PLH} t_{PHL}	0,55	1,70	0,60	1,70	0,65	1,80	ns	
S_n to output	t_{PLH} t_{PHL}	1,10	2,60	1,10	2,60	1,20	2,90	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,50	1,75	0,50	1,70	0,50	1,70	ns	

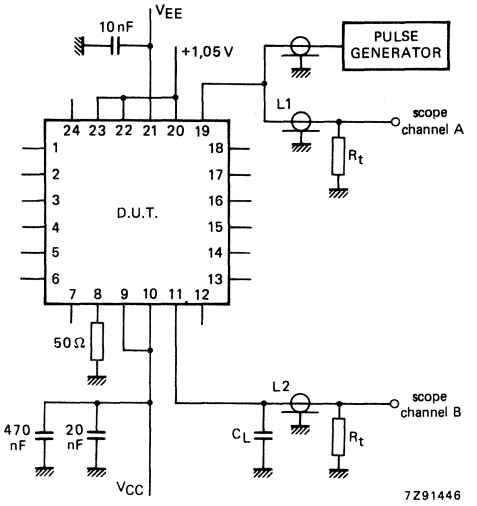


Fig. 3 A.C. test circuit.

Notes:

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope;
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown for flat pack, for slim cerdip package see Fig. 2.

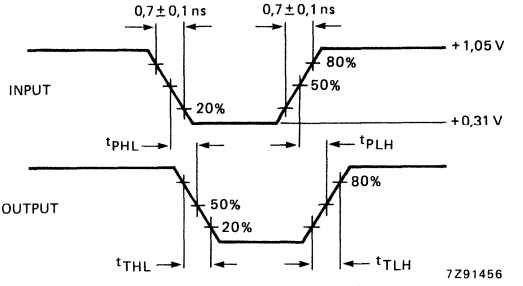


Fig. 4 Propagation delay and transition times.

16-BIT MULTIPLEXER

The 100164 output data (Q) is selected from one of sixteen data inputs (D_n). Selection is made using a 4-bit address (S_0 to S_3). Polarity of the data is unchanged.

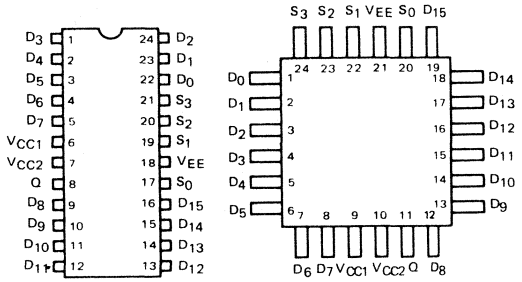


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	tp	typ.	1,6 ns
Power consumption per package	P_{av}	typ.	320 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100164Y: 24-lead flat-pack; ceramic (SOT-138)
100164F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

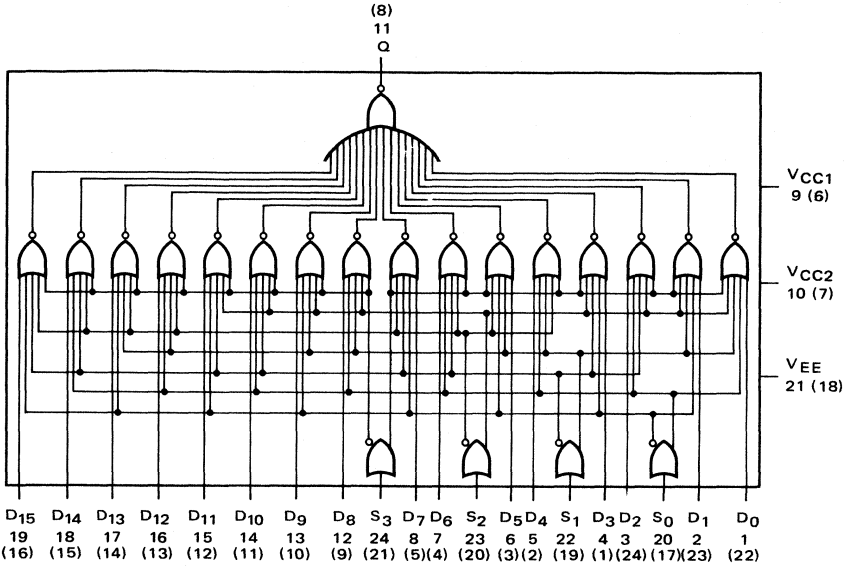


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP packages are between brackets.

TRUTH TABLE

address				data output
S_3	S_2	S_1	S_0	Q
L	L	L	L	D_0
L	L	L	H	D_1
L	L	H	L	D_2
L	L	H	H	D_3
L	H	L	L	D_4
L	H	L	H	D_5
L	H	H	L	D_6
L	H	H	H	D_7
H	L	L	L	D_8
H	L	L	H	D_9
H	L	H	L	D_{10}
H	L	H	H	D_{11}
H	H	L	L	D_{12}
H	H	L	H	D_{13}
H	H	H	L	D_{14}
H	H	H	H	D_{15}

H = HIGH level L = LOW level x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
D_n	I_{IH}	–	–	280	μA	$V_{in} = V_{IHmax}$
S_0, S_1, S_2, S_3	I_{IH}	–	–	240	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	49	71	105	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	0,80	2,20	0,90	2,35	0,90	2,55	ns	see Figs 3 and 4
S_0, S_1 to output	t_{PLH} t_{PHL}	1,45	3,20	1,45	3,20	1,45	3,60	ns	
S_2, S_3 to output	t_{PLH} t_{PHL}	1,10	2,50	1,10	2,50	1,10	2,80	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to output	t_{PLH} t_{PHL}	0,80	2,00	0,90	2,15	0,90	2,35	ns	see Figs 3 and 4
S_0, S_1 to output	t_{PLH} t_{PHL}	1,45	3,00	1,45	3,00	1,45	2,40	ns	
S_2, S_3 to output	t_{PLH} t_{PHL}	1,10	2,30	1,10	2,30	1,10	2,60	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

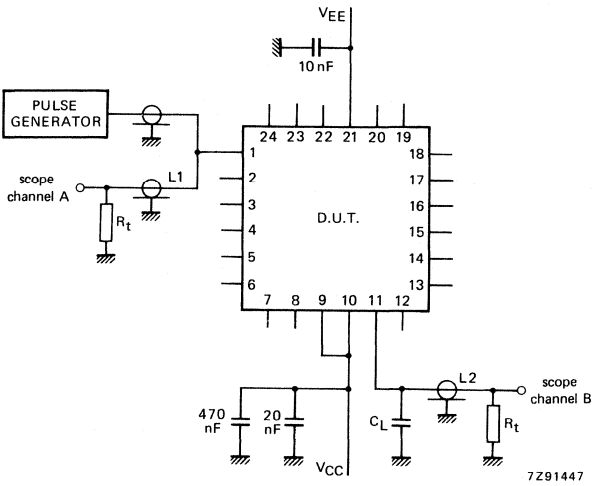


Fig. 3 A.C. test circuit.

Notes:

$V_{CC1} = V_{CC2} = 2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope;
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for flat pack, for slim cerdip package see Fig. 2.

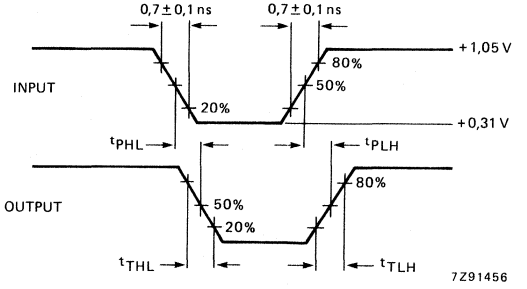


Fig. 4 Propagation delay and transition times.

UNIVERSAL PRIORITY ENCODER

100165 operates as a dual, 4-input or single, 8-input encoder, the operating mode is set by the mode control input (M). The eight data inputs (D_n) are latched and have a common enable ($\overline{E}$). The highest data priority, determined by the position of a HIGH bit in the input data group, is encoded to give a binary address from the outputs (Q_n). Complementary outputs ($\overline{Q}_n$) are also provided. In the dual mode, two groups of four inputs are encoded to give two 2-bit binary outputs, together with group signal outputs (GS_1, GS_2) which indicate that all bits of a data group are LOW. In the single mode, one group of eight inputs is encoded to give a 4-bit binary output together with a group signal (GS_2) which indicates that all bits of the input data are LOW. The output enable signal ($\overline{OE}$), when HIGH, forces all Q outputs LOW and all $\overline{Q}$ and GS outputs HIGH.
Expansion into other 100165 encoders can be made by connecting the relevant group signal output of one IC into the output enable input of the next.

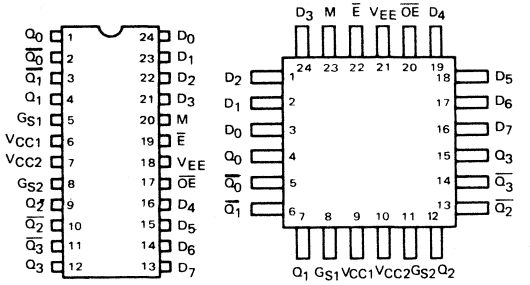


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	tp	typ.	2,5 ns
Power consumption per package	P_{av}	typ.	560 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100165Y: 24-lead flat-pack; ceramic (SOT-138).
100165F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

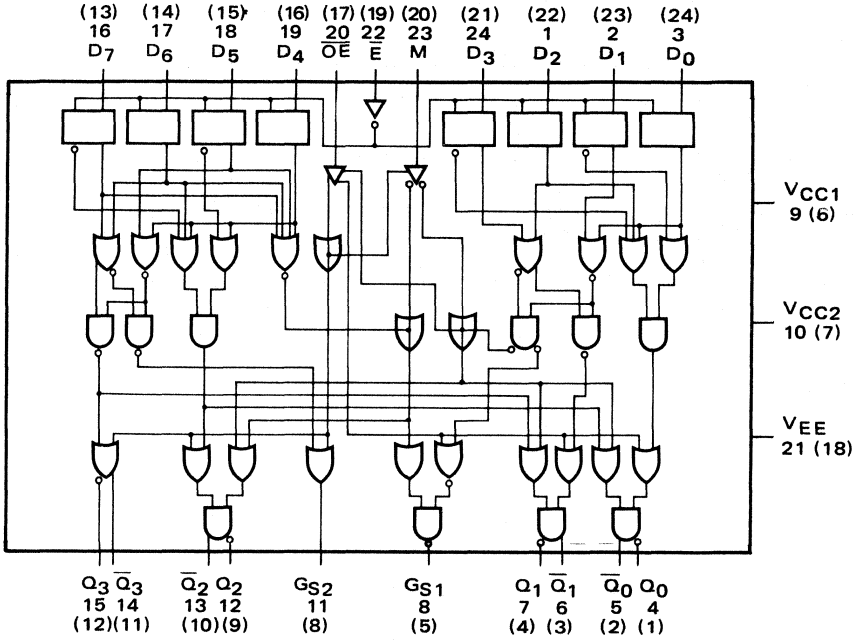


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

TRUTH TABLE

INPUTS											OUTPUTS					
$\overline{E}$	$\overline{OE}$	M	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	x	x	x					L	L			H	
L	L	L	L	H	x	x					H	L			H	
L	L	L	L	L	H	x					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	x	x	x			L	L		H
L	L	L					L	H	x	x			H	L		H
L	L	L					L	L	H	x			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	x	x	x	x	x	x	x	L	L	L	L	H	H
L	L	H	L	H	x	x	x	x	x	x	H	L	L	L	H	H
L	L	H	L	L	H	x	x	x	x	x	L	H	L	L	H	H
L	L	H	L	L	L	H	x	x	x	x	H	H	L	L	H	H
L	L	H	L	L	L	L	H	x	x	x	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	x	x	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	x	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
x	H	x	x	x	x	x	x	x	x	x	L	L	L	L	H	H
H	L	L									binary value from data before $\overline{E}$ changed L to H					
H	L	H														

H = HIGH level
L = LOW level
x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH	I_{IH}	–	–	230	μA	$V_{in} = V_{IHmax}$
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	77	125	200	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,10	4,10	1,10	4,10	1,10	4,60	ns	see Figs 3 and 4
D_n to GS	t_{PLH} t_{PHL}	1,10	4,10	1,10	4,10	1,10	4,40	ns	
$\overline{OE}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,00	3,30	1,00	3,30	1,00	3.40	ns	
$\overline{OE}$ to GS	t_{PLH} t_{PHL}	1,00	3,30	1,00	3,30	1,00	3,40	ns	see Figs 3 and 5
M to Q, $\overline{Q}$	t_{PLH} t_{PHL}	0,90	3,60	1,00	3,60	1,00	3,80	ns	
$\overline{E}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,40	4,70	1,40	4,60	1,40	5,00	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,40	0,45	1,40	ns	see Figs 3, 4 and 5
Set-up time D_n	t_s	1,10	–	1,00	–	1,10	–	ns	see Fig. 6
Hold time D_n	t_h	1,30	–	1,30	–	1,30	–	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_n to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,10	3,90	1,10	3,90	1,10	4,40	ns	see Figs 3 and 4
D_n to GS	t_{PLH} t_{PHL}	1,10	3,90	1,10	3,90	1,10	4,20	ns	
$\overline{OE}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,00	3,10	1,00	3,10	1,00	3,20	ns	
$\overline{OE}$ to GS	t_{PLH} t_{PHL}	1,00	3,10	1,00	3,10	1,00	3,20	ns	See Figs 3 and 5
M to Q, $\overline{Q}$	t_{PLH} t_{PHL}	0,90	3,40	1,00	3,40	1,00	3,60	ns	
$\overline{E}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1,40	4,50	1,40	4,40	1,40	4,80	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,45	1,40	0,45	1,40	0,45	1,40	ns	see Figs 3, 4 and 5
Set-up time D_n	t_s	0,90	–	0,80	–	0,90	–	ns	see Fig. 6
Hold time D_n	t_h	1,10	–	1,10	–	1,10	–	ns	

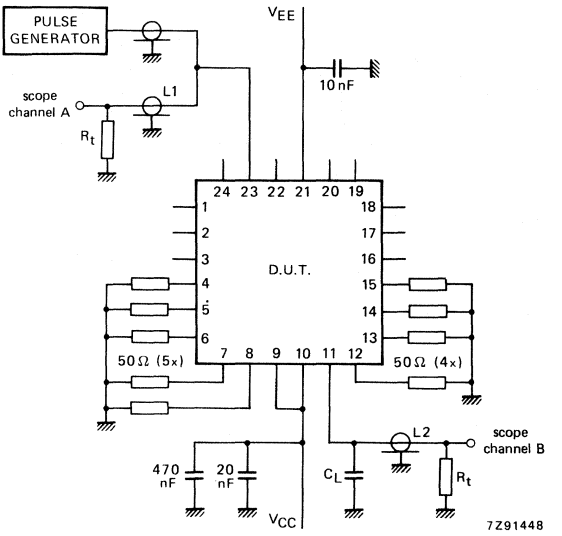


Fig. 3 A.C. test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} to V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for FLAT PACK. For slim cerdip package see logic symbol.

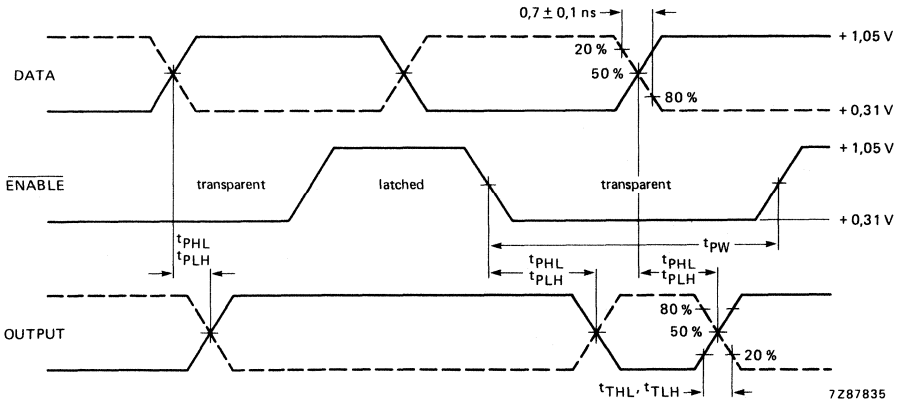


Fig. 4 Enable timing, propagation delay.

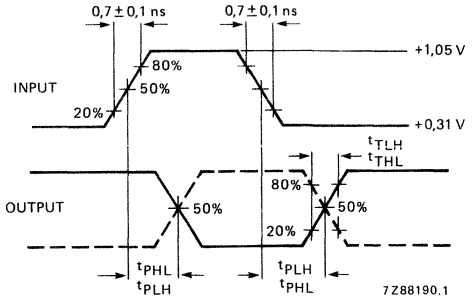


Fig. 5 Propagation delay (M, OE) and transition times.

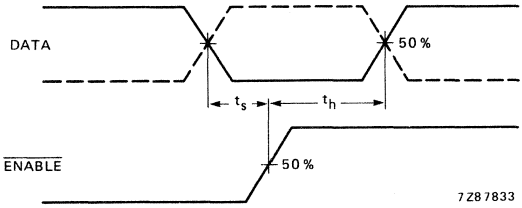


Fig. 6 Set-up and hold time.

Notes t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

9-BIT COMPARATOR

The 100166 compares the arithmetic values of two 9-bit words and indicates whether the value of one word is equal to or greater than that of the other.

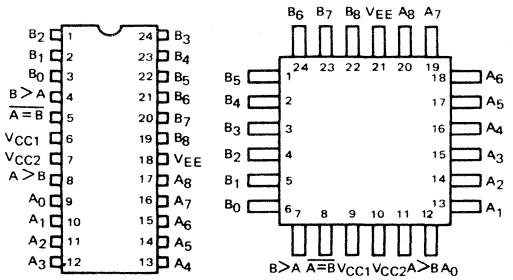


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	t_P	typ.	2,3 ns
Power consumption per package	P_{av}	typ.	630 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100166Y: 24-lead flat-pack; ceramic (SOT-138)
100166F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

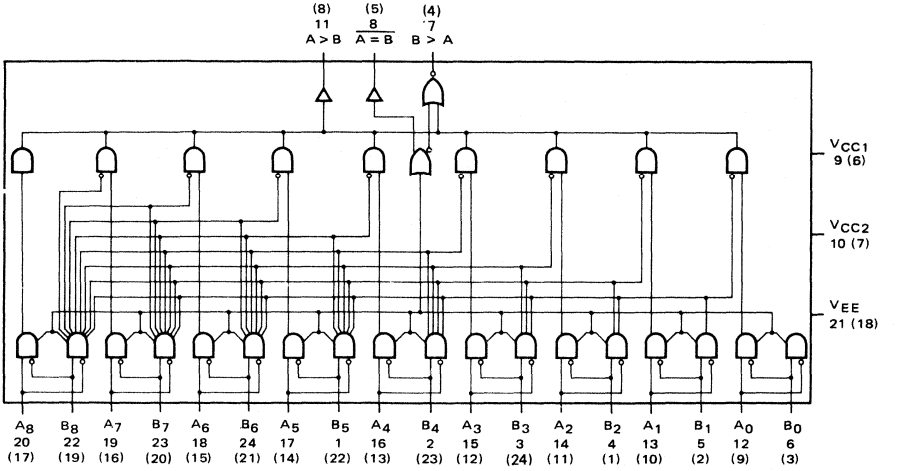


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

TRUTH TABLE

INPUTS																OUTPUTS		
A_8	B_8	A_7	B_7	A_6	B_6	A_5	B_5	A_4	B_4	A_3	B_3	A_2	B_2	A_1	B_1	A_0	B_0	A>B	B>A	A=B
H	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	H
L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H
A=B		H	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	H	L	H
A=B		L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H
A=B		A=B		H	L	—	—	—	—	—	—	—	—	—	—	—	—	H	L	H
A=B		A=B		L	H	—	—	—	—	—	—	—	—	—	—	—	—	L	H	H
A=B		A=B		A=B		H	L	—	—	—	—	—	—	—	—	—	—	H	L	H
A=B		A=B		A=B		L	H	—	—	—	—	—	—	—	—	—	—	L	H	H
A=B		A=B		A=B		A=B		H	L	—	—	—	—	—	—	—	—	H	L	H
A=B		A=B		A=B		A=B		L	H	—	—	—	—	—	—	—	—	L	H	H
A=B		A=B		A=B		A=B		A=B		H	L	—	—	—	—	—	—	H	L	H
A=B		A=B		A=B		A=B		A=B		L	H	—	—	—	—	—	—	L	H	H
A=B		A=B		A=B		A=B		A=B		A=B		H	L	—	—	—	—	H	L	H
A=B		A=B		A=B		A=B		A=B		A=B		L	H	—	—	—	—	L	H	H
A=B		A=B		A=B		A=B		A=B		A=B		A=B		H	L	—	—	H	L	H
A=B		A=B		A=B		A=B		A=B		A=B		A=B		L	H	—	—	L	H	H
A=B		A=B		A=B		A=B		A=B		A=B		A=B		A=B		H	L	H	L	H
A=B		A=B		A=B		A=B		A=B		A=B		A=B		A=B		L	H	L	H	H
A=B		A=B		A=B		A=B		A=B		A=B		A=B		A=B		A=B		L	L	L

H = HIGH level L = LOW level x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH	I_{IH}	—	—	250	μA	V_{in} = V_{IHmax}
Input current LOW	I_{IL}	0,5	—	—	μA	V_{in} = V_{ILmin}
Supply current	$-I_{EE}$	119	140	238	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay Data to output	t_{PLH} t_{PHL}	1,40	3,80	1,40	3,80	1,40	3,90	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay Data to output	t_{PLH} t_{PHL}	1,40	3,60	1,40	3,60	1,40	3,70	ns	see Figs 3 and 4
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

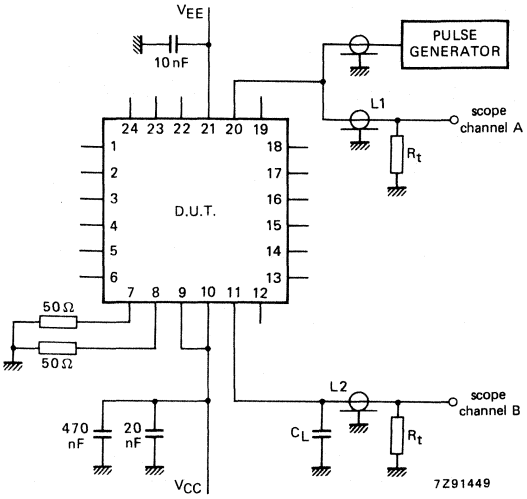


Fig. 3 A.C. test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for flat pack, for slim cerdip package see Fig. 2.

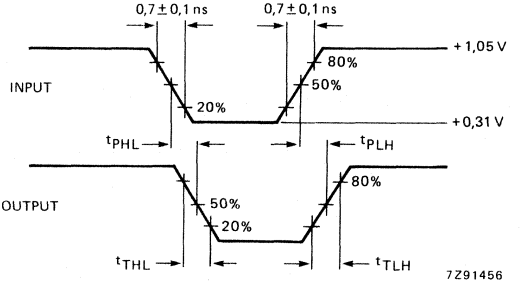


Fig. 4 Propagation delay and transition times.

UNIVERSAL DEMULTIPLEXER/DECODER

The 100170 operates as a dual 1-of-4 decoder or as a single 1-of-8 decoder; the operating mode being fixed by the mode control input (M). The decoder outputs (Q_n) can be active HIGH or active LOW as determined by the inputs H_a, H_b and H_c. Two enable inputs ($\overline{E}_1$, $\overline{E}_2$) are provided for each 1-of-4 decoder; the pinning is arranged so that pairs of enables can be conveniently tied together for the 1-of-8 decoder mode (pins 19/20, 22/23 (slim cerdip package) or pins 16/17, 19/20 (flat pack package).

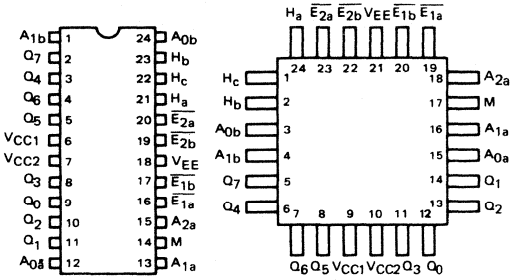


Fig. 1 Pin designation: slim cerdip and flat pack package.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay (DATA, ADDRESS)	tp	typ.	1.8 ns
Power consumption per package	P_{av}	typ.	495 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100170Y: 24-lead flat-pack; ceramic (SOT-138)
100170F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)

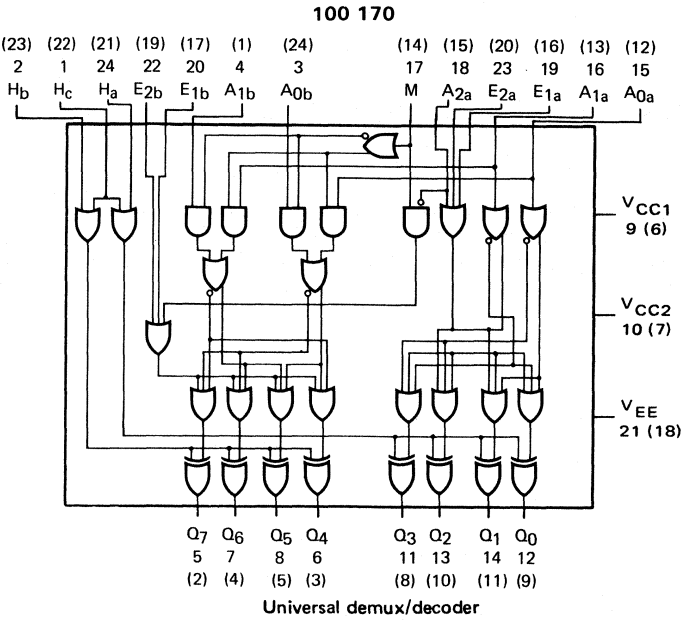


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP packages are between brackets.

TRUTH TABLES

Dual 1-of-4 decoder mode: M = A_{2a} = H_c = LOW

inputs				outputs (H_a=H_b=HIGH)				outputs (H_a = H_b = LOW)			
$\overline{E}_1$	$\overline{E}_2$	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_0	Q_1	Q_2	Q_3
H	x	x	x	L	L	L	L	H	H	H	H
x	H	x	x	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	L	H	H	H	L

Dual 1-of-8 decoder mode: M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW

inputs					outputs (H_c = HIGH)								outputs (H_c = LOW)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
H	x	x	x	x	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
x	H	x	x	x	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	L	H	L	L	L	L	L	L	H	L	H	H	H	H	H	H
L	L	L	H	L	L	L	H	L	L	L	L	L	H	H	L	H	H	H	H	H
L	L	L	H	H	L	L	L	H	L	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	L	L	L	L	H	L	L	L	H	H	H	H	L	H	L	H
L	L	H	L	H	L	L	L	L	L	H	L	L	H	H	H	H	H	L	H	H
L	L	H	H	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L

H = HIGH level L = LOW level x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
H_c, A_{0a}, A_{1a}, A_{2a}	I_{IH}	–	–	310	μA	V_{in} = V_{IHmax}
all other inputs	I_{IH}	–	–	250	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	V_{in} = V_{ILmin}
Supply current	$-I_{EE}$	76	110	153	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; V_{CC1} = V_{CC2} = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
E_{na},E_{nb} to output	t_{PLH} t_{PHL}	0,80	2,30	0,80	2,20	0,80	2,30	ns	
A_{na},A_{nb} to output	t_{PLH} t_{PHL}	0,95	2,80	0,95	2,70	1,00	2,90	ns	
H_a,H_b,H_c to output	t_{PLH} t_{PHL}	1,00	3,00	1,00	2,90	1,00	3,00	ns	see Figs 3 and 4
M to output	t_{PLH} t_{PHL}	1,50	3,90	1,60	3,80	1,60	3,90	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

FLAT PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
E_{na},E_{nb} to output	t_{PLH} t_{PHL}	0,80	2,10	0,80	2,00	0,80	2,10	ns	
A_{na},A_{nb} to output	t_{PLH} t_{PHL}	0,95	2,60	0,95	2,50	1,00	2,70	ns	
H_a,H_b,H_c to output	t_{PLH} t_{PHL}	1,00	2,80	1,00	2,70	1,00	2,80	ns	see Figs 3 and 4
M to output	t_{PLH} t_{PHL}	1,50	3,70	1,60	3,60	1,60	3,70	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,60	0,45	1,60	0,45	1,60	ns	

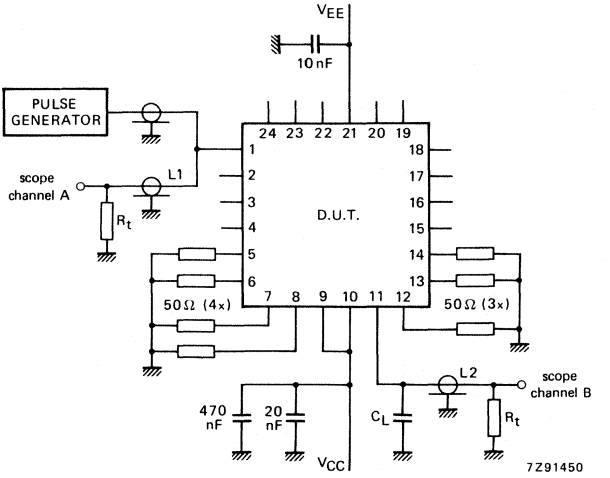


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for FLAT PACK. For dual-in-line package see logic diagram.

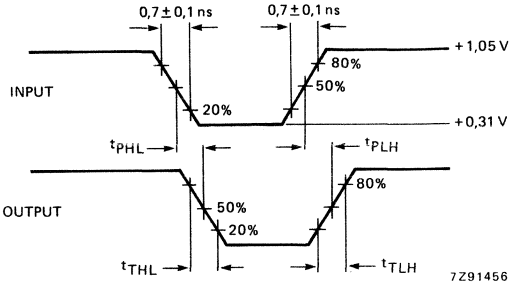


Fig. 4 Propagation delay and transition times.

TRIPLE 4-INPUT MULTIPLEXER

The 100171 has three 4-input multiplexers with common decoding and enable. The decoder is controlled by inputs S_0 and S_1 and selects one bit from each of the data inputs. True and complement outputs are available from each multiplexer. A HIGH on the enable input $\overline{E}$ drives all true outputs LOW and complement outputs HIGH.

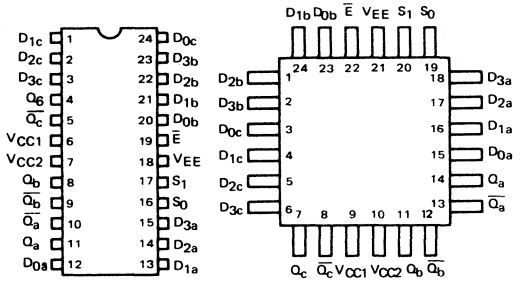


Fig. 1 Pin designation: slim cerdip and flat pack packages.

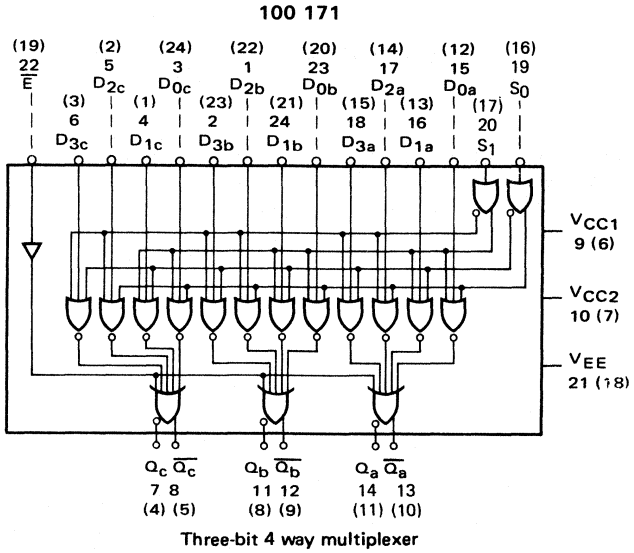
QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	tp	typ.	1,1 ns
Power consumption per package	P_{av}	typ.	370 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100171Y: 24-lead flat-pack; ceramic (SOT-138)
100171F: 24-lead dual in-line; ceramic (cerdip) (SOT-149)



Three-bit 4 way multiplexer

Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP package are between brackets.

TRUTH TABLE

enable	select		data inputs				outputs	
$\overline{E}$	S_1	S_0	D_0	D_1	D_2	D_3	$\overline{Q}$	Q
H	x	x	x	x	x	x	H	L
L	L	L	L	x	x	x	H	L
L	L	L	H	x	x	x	L	H
L	L	H	x	L	x	x	H	L
L	L	H	x	H	x	x	L	H
L	H	L	x	x	L	x	H	L
L	H	L	x	x	H	x	L	H
L	H	H	x	x	x	L	H	L
L	H	H	x	x	x	H	L	H

H = HIGH level
L = LOW level
x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
D_{nx}	I_{IH}	–	–	340	μA	$V_{in} = V_{IHmax}$
$S_0, S_1, \overline{E}$	I_{IH}	–	–	300	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	56	83	114	mA	Inputs open

A.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{nx} to output	t_{PLH} t_{PHL}	0,45	1,70	0,45	1,60	0,50	1,70	ns	
S_0, S_1 to output	t_{PLH} t_{PHL}	0,90	2,80	0,90	2,80	1,00	3,00	ns	see Figs 3 and 4
$\overline{E}$ to output	t_{PLH} t_{PHL}	0,65	2,60	0,65	2,60	0,75	2,90	ns	
Transition time	t_{TLH} t_{THL}	0,45	1,70	0,45	1,50	0,45	1,50	ns	

FLAT PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
D_{nx} to output	t_{PLH} t_{PHL}	0,45	1,50	0,45	1,40	0,50	1,50	ns	
S_0, S_1 to output	t_{PLH} t_{PHL}	0,90	2,60	0,90	2,60	1,00	2,80	ns	see Figs 3 and 4
$\overline{E}$ to output	t_{PLH} t_{PHL}	0,65	2,40	0,65	2,40	0,75	2,70	ns	
Transition time	t_{THL} t_{THL}	0,45	1,70	0,45	1,50	0,45	1,50	ns	

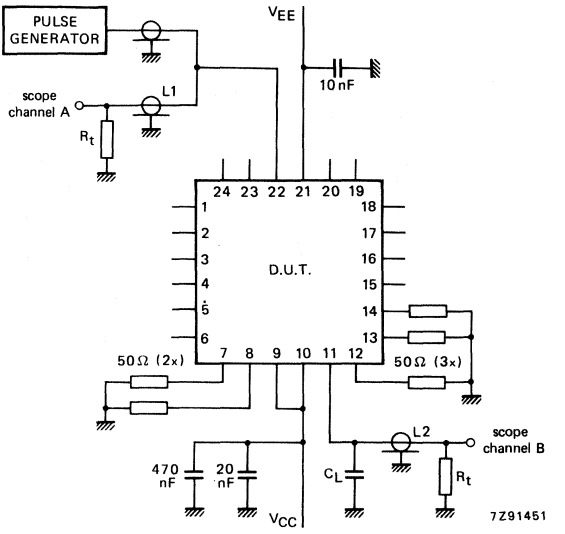


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic diagram.

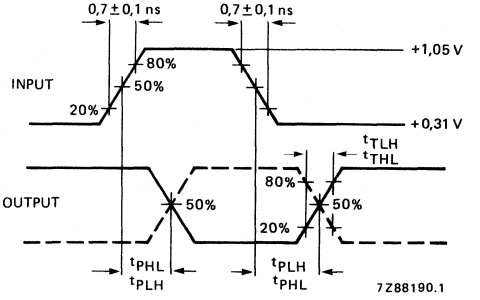


Fig. 4 Propagation delay and transition times.

QUINTUPLE LATCH: ECL 100.000 INPUTS; ECL10.000 OUTPUTS

The 100175 has five latches, each with one data input (D_n) and one data output (Q_n). Clear input (C) and enable inputs ($\overline{E_1}$ and $\overline{E_2}$) are common to all latches. Each Q output follows the state of its D input when $\overline{E_1}$ and $\overline{E_2}$ are LOW. The latches store the last valid data present at their D input when Either or both $\overline{E_1}$ and $\overline{E_2}$ are HIGH, and a HIGH at the C input takes the Q outputs LOW when either or both $\overline{E_1}$ and $\overline{E_2}$ are HIGH. All inputs are compatible with devices of the ECL100.000 series and all outputs are compatible with those of the ECL10.000 series.

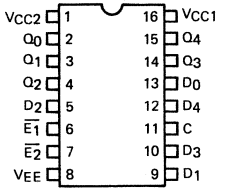


Fig. 1 Pin designation.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−5,2 V
Operating ambient temperature	T_{amb}		0 to +75 °C
Average propagation delay			
DATA	t_P	typ.	2,2 ns
ENABLE	t_P	typ.	2,7 ns
Power consumption per package	P_{av}	typ.	350 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100175D: 16-lead dual in-line; ceramic (cerdip) (SOT-74A).

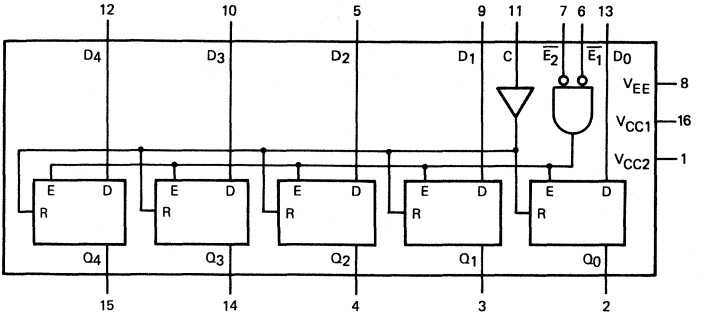


Fig. 2 Logic diagram

TRUTH TABLE

D_n	$\overline{E_1}$	$\overline{E_2}$	C	Q_n
H	L	L	x	H
L	L	L	x	L
x	H	x	L	no change
x	x	H	L	no change
x	H	x	H	L
x	x	H	H	L

H = HIGH level voltage
L = LOW level voltage
x = Don't care

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = –5.2 V; V_{CC1} = V_{CC2} = ground; T_{amb} = 0 to +75°C; unless otherwise specified

description	symbol	0°C		25°C		75°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Output voltage HIGH	V_{OH}	–1000	– 840	– 960	– 810	– 900	– 720	mV	V_{in} = V_{IHmax} or V_{ILmin}
Output voltage LOW	V_{OL}	–1870	–1665	–1850	–1650	–1830	–1625	mV	V_{in} = V_{IHmax} or V_{ILmin}
Output voltage HIGH	V_{OHC}	–1020	–	– 980	–	– 920	–	mV	V_{in} = V_{IHmin} or V_{ILmax}
Output voltage LOW	V_{OLC}	–	–1645	–	–1630	–	–1605	mV	V_{in} = V_{IHmin} or V_{IHmax}
Input current HIGH									
carry input C	I_{IH}	–	650	–	650	–	650	μA	V_{in} =
other inputs	I_{IH}	–	290	–	290	–	290	μA	V_{IHmax}
Input current LOW	I_{IL}	0,5	–	0,5	–	0,5	–	μA	V_{in} = V_{ILmin}
Supply current	$-I_{EE}$	50	102	50	102	50	102	mA	inputs open Typical value = 67 mA

A.C. CHARACTERISTICS

V_{EE} = –5,2 V; V_{CC1} = V_{CC2} = ground

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay D_n to Q_n	t_{PLH} t_{PHL}	1,00	3,40	1,00	3,40	1,00	3,40	ns	see Figs 3 and 4
Propagation delay $\overline{E_1}$, $\overline{E_2}$ to Q	t_{PLH} t_{PHL}	1,00	4,30	1,00	4,30	1,00	4,30	ns	see Figs 3 and 5
Propagation delay C to Q	t_{PLH} t_{PHL}	1,00	3,90	1,00	3,90	1,00	3,90	ns	see Figs 3, 4 and 5
Transition time	t_{TLH} t_{THL}	0,90	3,50	1,00	3,50	0,90	3,50	ns	see Figs 3, 4 and 5
Set-up time D_n	t_s	2,5	–	2,5	–	2,5	–	ns	see Fig. 6
Hold time D_n	t_h	0,5	–	0,5	–	0,5	–	ns	see Fig. 7

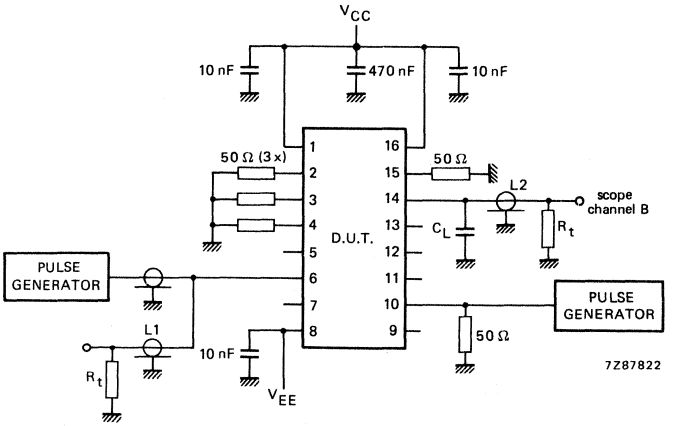


Fig. 3 Switching time test circuit.

Notes:

V_{CC1} = V_{CC2} = 2 V; V_{EE} = –2,5 V;
L_1 = L_2 = 50 Ω impedance lines of equal length;
R_t = 50 Ω termination to scope;
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixuture + stray capacitance ⩽ 3 pF;
All unused outputs are loaded with 50 Ω to ground.

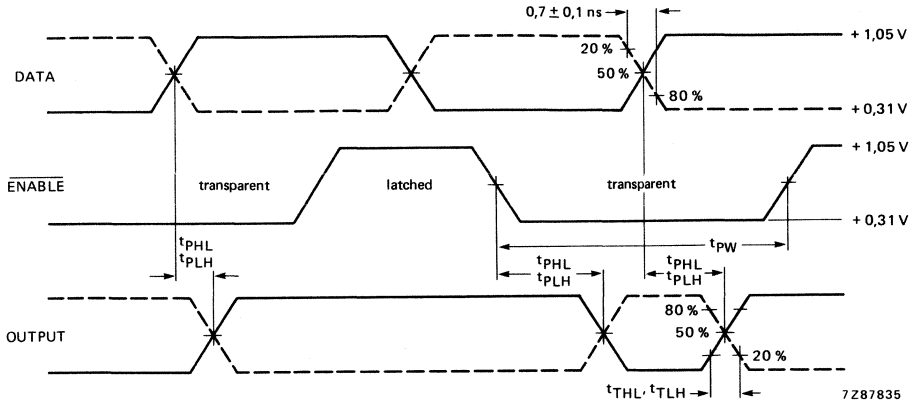


Fig. 4 Enable timing.

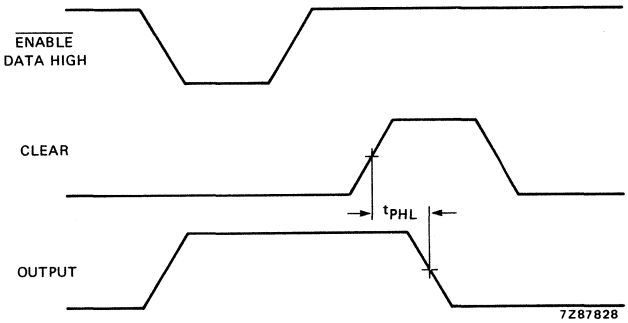


Fig. 5 Clear timing (data HIGH).

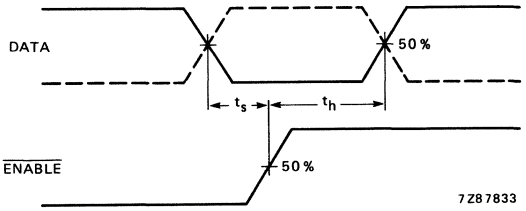


Fig. 6 Data set-up and hold times.

Notes t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

FAST 6-BIT ADDER

10080 is a high-speed adder which performs a full addition of two 6-bit operants in 2 ns. The inputs are Carry ($\overline{CN}$) (active LOW), Operands A (A_0 to A_5) and Operands B (B_0 to B_5). The outputs are Function (F_0 to F_5), Carry-generate ($\overline{G}$) (active LOW) and Carry-propagate ($\overline{P}$) (active LOW).

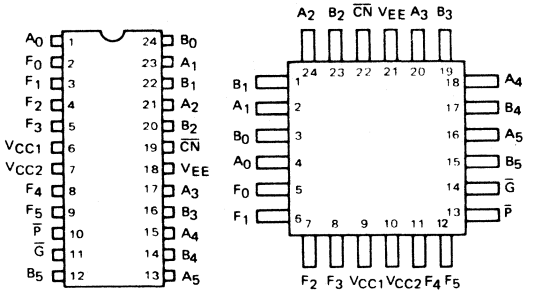


Fig. 1 Pin designation: slim cerdip and flat pack package.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay	tp		2,35 ns
Power consumption per package	P_{av}	typ.	920 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100180Y: 24-lead flat-pack; ceramic (SOT-138).
100180F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

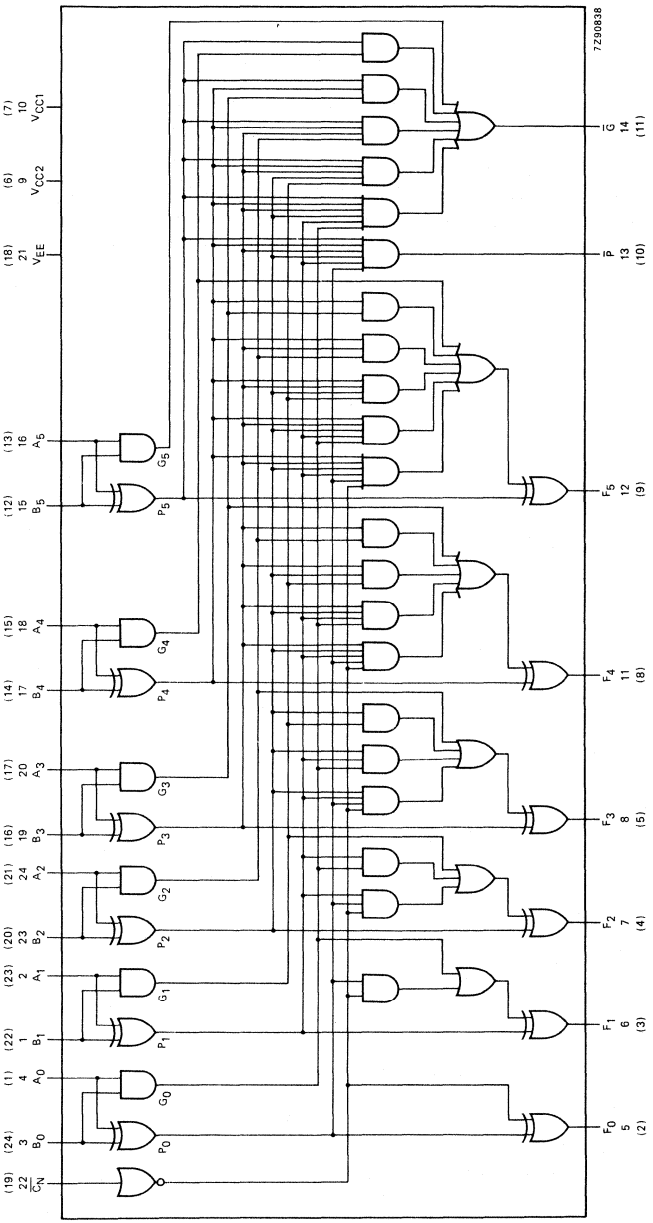


Fig. 2 Logic diagram. Pin numbers for SLIM CERDIP packages are between brackets.

LOGIC EQUATIONS

$F_0 = P_0 \oplus C_N$

$F_1 = P_1 \oplus (G_0 + P_0\, C_N)$

$F_2 = P_2 \oplus (G_1 + P_1\, G_0 + P_1\, P_0\, C_N)$

$F_3 = P_3 \oplus (G_2 + P_2\, G_1 + P_2\, P_1\, G_0 + P_2\, P_1\, P_0\, C_N)$

$F_4 = P_4 \oplus (G_3 + P_3\, G_2 + P_3\, P_2\, G_1 + P_3\, P_2\, P_1\, G_0 + P_3\, P_2\, P_1\, P_0\, C_N)$

$F_5 = P_5 \oplus (G_4 + P_4\, G_3 + P_4\, P_3\, G_2 + P_4\, P_3\, P_2\, G_1 + P_4\, P_3\, P_2\, P_1\, G_0 + P_4\, P_3\, P_2\, P_1\, P_0\, C_N)$

$\overline{P} = \overline{P_0\, P_1\, P_2\, P_3\, P_4\, P_5}$

$\overline{G} = \overline{G_5 + P_5\, G_4 + P_5\, P_4\, G_3 + P_5\, P_4\, P_3\, G_2 + P_5\, P_4\, P_3\, P_2\, G_1 + P_5\, P_4\, P_3\, P_2\, P_1\, G_0}$

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

($i = 0, 1, 2, 3, 4, 5$; $\oplus$ = exclusive OR)

RATINGS see Family Specifications

D.C. CHARACTERISTICS

$V_{ee} = -4{,}2$ to $-4{,}8$ V; $V_{CC1} = V_{CC2}$ = ground; $T_{amb} = 0$ to $+85^{o}$C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH	I_{IH}	–	–	220	μA	$V_{in} = V_{IHmax}$
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	135	205	290	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground; unless otherwise specified

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n, B_n to F_n	t_{PLH} t_{PHL}	1,10	4,70	1,10	4,60	1,10	4,70	ns	
A_n, B_n to $\overline{P}$	t_{PLH} t_{PHL}	1,00	3,00	1,00	3,00	1,00	3,30	ns	
A_n, B_n to $\overline{G}$	t_{PLH} t_{PHL}	1,10	3,90	1,20	3,80	1,20	3,90	ns	see Figs 3 and 4
$\overline{G}$ to F_n	t_{PLH} t_{PHL}	0,90	4,00	0,90	3,90	0,90	4,00	ns	
Transition time	t_{TLH} t_{THL}	0,45	2,30	0,45	2,20	0,45	2,30	ns	

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n, B_n to F_n	t_{PLH} t_{PHL}	1,10	4,50	1,10	4,40	1,10	4,50	ns	
A_n, B_n to $\overline{P}$	t_{PLH} t_{PHL}	1,00	2,80	1,00	2,80	1,00	3,10	ns	
A_n, B_n to $\overline{G}$	t_{PLH} t_{PHL}	1,10	3,70	1,20	3,60	1,20	3,70	ns	see Figs 3 and 4
$\overline{G}$ to F_n	t_{PLH} t_{PHL}	0,90	3,80	0,90	3,70	0,90	3,80	ns	
Transition time	t_{TLH} t_{THL}	0,45	2,30	0,45	2,20	0,45	2,30	ns	

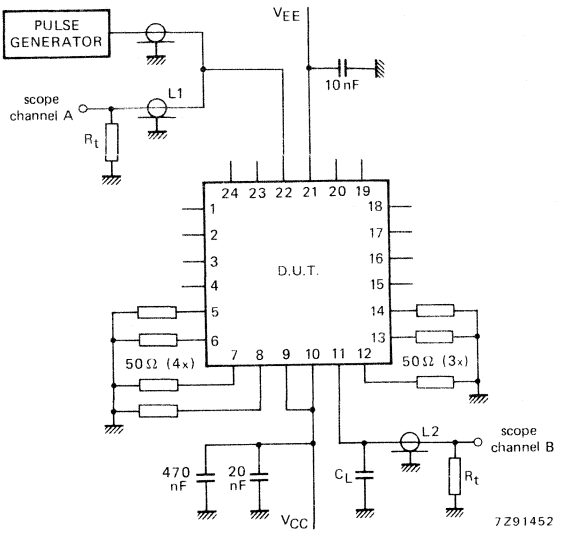


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic diagram.

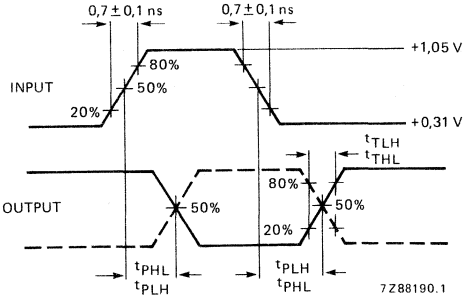


Fig. 4 Propagation delay and transition times.

4-BIT BINARY/BCD ALU

This 4-bit binary/BCD arithmetic logic unit performs eight logic an eight arithmetic functions on two 4-bit words (A_0 to A_3 and B_0 to B_3), giving binary/BCD addition and substraction and supplementary binary arithmetic. Functions are selected using a 4-bit binary code (S_0 to S_3).
Operating speed is increased by latched function outputs (F_0 to F_3) which are transparant when the enable input ($\overline{E}$) is LOW. An internal look-ahead-carry minimizes delay to the function outputs and to the ripple carry output ($\overline{C_N+4}$).
The group-carry-look-ahead-propagate output ($\overline{P}$) goes LOW when an add operation gives fifteen (binary) or nine (BCD), or when a subtract operation gives zero. The generate output ($\overline{G}$) goes LOW when the sum of words A and B is greater than fifteen (binary) or nine (BCD), or when the difference in a subtract function is not zero. Both $\overline{P}$ and $\overline{G}$ operate independently of the carry-in input $\overline{C_N}$. When $\overline{C_N}$ is LOW, BCD subtractions are performed in ten's complement or binary subtractions in one's complement.

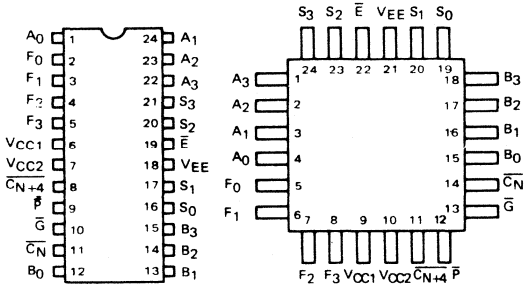


Fig. 1 Pin designation: slim cerdip and flat pack packages.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay E to F_n	tp		2,1 ns
Power consumption per package	P_{av}		920 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100181Y: 24-lead flat pack; ceramic (SOT-138).
100181F: 24-lead dual in-line; ceramic (cerdip) (SOT-149).

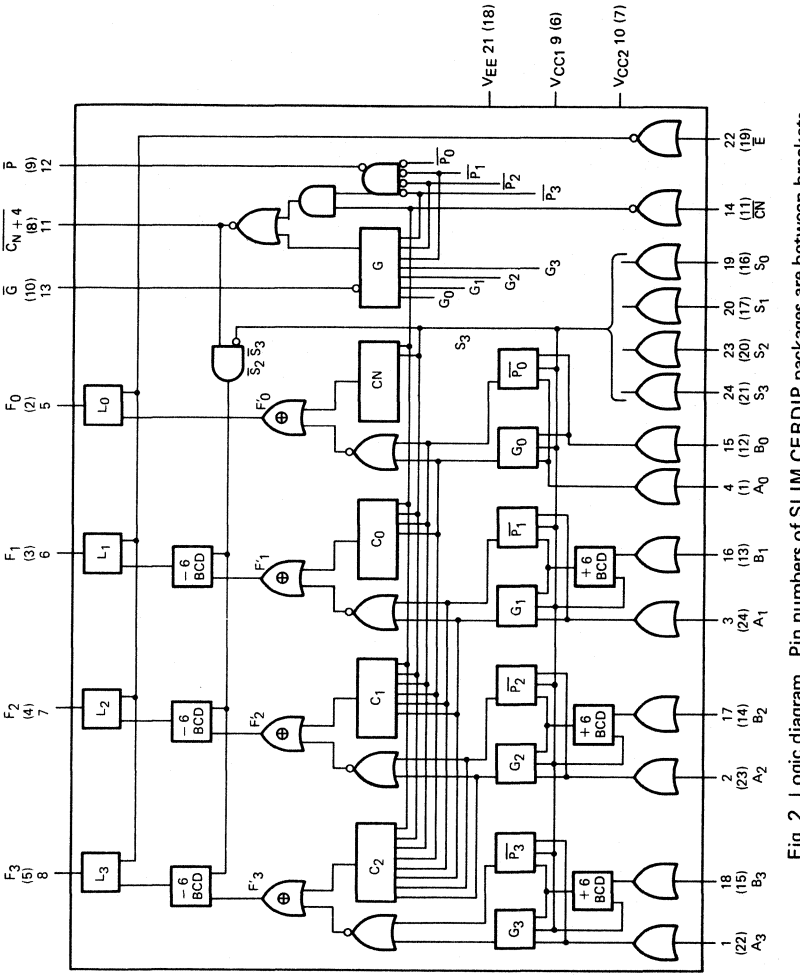


Fig. 2 Logic diagram. Pin numbers of SLIM CERDIP packages are between brackets.

TRUTH TABLE

selection				functions	
S_3	S_2	S_1	S_0	$\overline{C_N}$ = H	$\overline{C_N}$ = L
L	L	L	L	A + B (BCD)	A + B + 1 (BCD)
L	L	L	H	A − B (BCD)	A − B + 1 (BCD)
L	L	H	L	B − A (BCD)	B − A + 1 (BCD)
L	L	H	H	0 − B (BCD)	0 − B + 1 (BCD)
L	H	L	L	A + B (binary)	A + B + 1 (binary)
L	H	L	H	A − B (binary)	A − B + 1 (binary)
L	H	H	L	B − A (binary)	B − A + 1 (binary)
L	H	H	H	0 − B (binary)	0 − B + 1 (binary)
H	L	L	L	$F_n = A_nB_n + \overline{A_n}\overline{B_n}$	SAME LOGIC
H	L	L	H	$F_n = A_n\overline{B_n} + \overline{A_n}B_n$	
H	L	H	L	$F_n = A_n + B_n$	
H	L	H	H	$F_n = A_n$	
H	H	L	L	$F_n = \overline{B_n}$	
H	H	L	H	$F_n = B_n$	
H	H	H	L	$F_n = A_n . B_n$	
H	H	H	H	F_n = LOW	

H = HIGH voltage level
L = LOW voltage level

RATINGS see Family Specifications

D.C. CHARACTERISTICS

V_{EE} = −4,2 to −4,8 V; $V_{CC1} = V_{CC2}$ = ground; T_{amb} = 0 to +85°C; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
Input current HIGH						
S_n, $\overline{E}$	I_{IH}	–	–	350	μA	$V_{in} = V_{IHmax}$
all other signal pins	I_{IH}	–	–	250	μA	
Input current LOW	I_{IL}	0,5	–	–	μA	$V_{in} = V_{ILmin}$
Supply current	$-I_{EE}$	130	205	300	mA	inputs open

A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground; unless otherwise specified

DUAL IN-LINE PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n, B_n to F_n	t_{PLH} t_{PHL}	2,00	6,90	2,10	6,80	2,10	7,40	ns	
A_n, B_n to $\overline{P}$, $\overline{G}$	t_{PLH} t_{PHL}	1,40	4,70	1,40	4,40	1,40	4,70	ns	
A_n, B_n to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	2,00	6,50	2,00	6,50	2,10	6,80	ns	
$\overline{C_N}$ to F_n	t_{PLH} t_{PHL}	1,60	5,10	1,60	5,20	1,60	5,50	ns	see Figs 3 and 4
$\overline{C_N}$ to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	1,30	3,00	1,40	3,00	1,40	3,10	ns	see Figs 3 and 4
S_n to F_n	t_{PLH} t_{PHL}	1,40	8,80	1,50	8,60	1,50	9,00	ns	
S_n to $\overline{P}$, $\overline{G}$	t_{PLH} t_{PHL}	1,70	7,40	2,00	5,90	2,00	6,50	ns	
S_n to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	2,70	10,10	2,80	8,50	2,90	8,70	ns	
$\overline{E}$ to F_n	t_{PLH} t_{PHL}	1,00	3,40	0,90	3,60	1,10	3,80	ns	
Transition time	t_{TLH} t_{THL}	0,45	3,50	0,45	3,50	0,45	3,50	ns	
Set-up time A_n, B_n	t_s	7,70	–	7,70	–	8,20	–	ns	
Set-up time S_n	t_s	8,80	–	8,60	–	9,70	–	ns	
Set-up time $\overline{C_N}$	t_s	4,90	–	5,10	–	5,40	–	ns	
Hold time A_n, B_n	t_h	0,20	–	0,20	–	0,20	–	ns	see Fig. 5
Hold time S_n	t_h	0,70	–	0,70	–	0,70	–	ns	
Hold time $\overline{C_N}$	t_h	0,70	–	0,70	–	0,70	–	ns	
Pulse width LOW $\overline{E}$	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Fig. 4

FLAT PACK PACKAGE

description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
A_n, B_n to F_n	t_{PLH} t_{PHL}	2,00	6,70	2,10	6,60	2,10	7,20	ns	
A_n, B_n to $\overline{P}$, $\overline{G}$	t_{PLH} t_{PHL}	1,40	4,50	1,40	4,20	1,40	4,50	ns	
A_n, B_n to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	2,00	6,30	2,00	6,30	2,10	6,60	ns	
$\overline{C_N}$ to F_n	t_{PLH} t_{PHL}	1,60	4,90	1,60	5,00	1,60	5,30	ns	see Figs 3 and 4
$\overline{C_N}$ to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	1,30	2,80	1,40	2,80	1,40	2,90	ns	
S_n to F_n	t_{PLH} t_{PHL}	1,40	8,60	1,50	8,40	1,50	8,80	ns	
S_n to $\overline{P}$, $\overline{G}$	t_{PLH} t_{PHL}	1,70	7,20	2,00	5,70	2,00	6,30	ns	
S_n to $\overline{C_{N+4}}$	t_{PLH} t_{PHL}	2,70	9,90	2,80	8,30	2,90	8,50	ns	
$\overline{E}$ to F_n	t_{PLH} t_{PHL}	1,00	3,20	0,90	3,40	1,10	3,60	ns	
Transition time	t_{TLH} t_{THL}	0,45	3,50	0,45	3,50	0,45	3,50	ns	
Set-up time A_n, B_n	t_s	7,50	–	7,50	–	8,00	–	ns	
Set-up time S_n	t_s	8,60	–	8,40	–	9,50	–	ns	
Set-up time $\overline{C_N}$	t_s	4,70	–	4,90	–	5,20	–	ns	see Fig. 5
Hold time A_n, B_n	t_h	0,00	–	0,00	–	0,00	–	ns	
Hold time S_n	t_h	0,50	–	0,50	–	0,50	–	ns	
Hold time $\overline{C_N}$	t_h	0,50	–	0,50	–	0,50	–	ns	
Pulse width LOW $\overline{E}$	$t_{PW(H)}$	2,50	–	2,50	–	2,50	–	ns	see Fig. 4

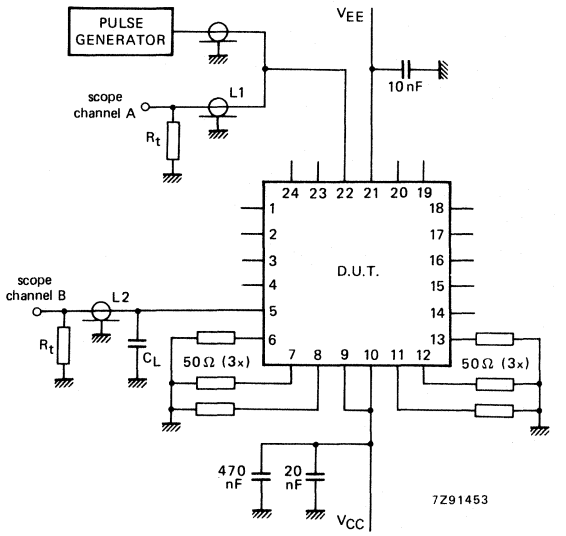


Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{EE} = -2{,}5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF;
All unused outputs are loaded with 50 Ω to ground.
Pin numbers shown are for FLAT PACK. For dual in-line package see logic diagram.

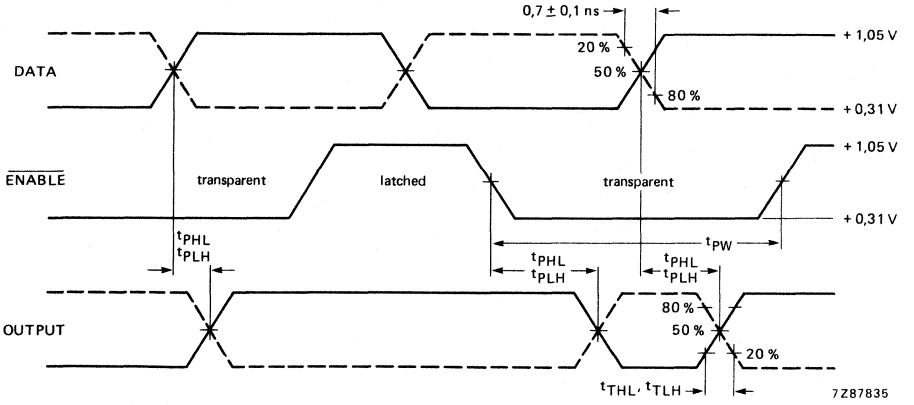


Fig. 4 Enable timing.

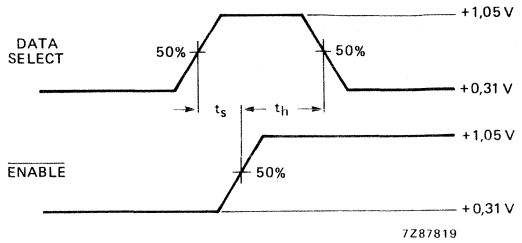


Fig. 5 Data set-up and hold time.

Notes: t_s is the minimum time **before** the transition of the clock that information must be present at the data input.

t_h is the minimum time **after** the transition of the clock that information must remain unchanged at the data input.

ECL 100.000 TO TTL INTERFACE

The 100255 is a quintuple, bidirectional ECL to TTL translating interface. The ECL inputs/outputs (I/O_{En}) are compatible with all devices of the ECL100.000 series and the input/outputs (I/O_{Tn}) are TTL compatible. A mode control input (M) selects the direction of translation and a chip enable input ($\overline{CE}$) enables the translation (M and $\overline{CE}$ are ECL inputs).

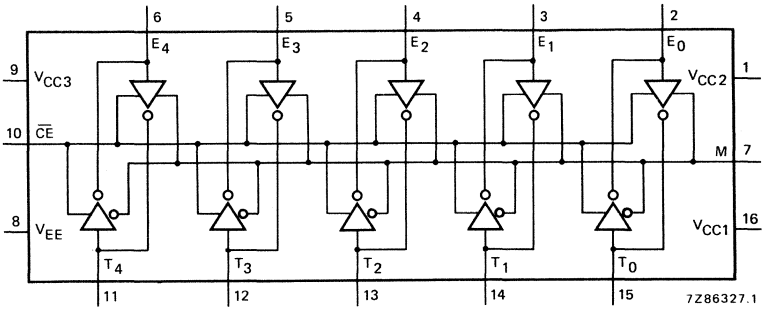


Fig. 1 Logic diagram.

QUICK REFERENCE DATA

Supply voltage	V_{EE}	typ.	−4,5 V
Operating ambient temperature	T_{amb}		0 to +85 °C
Average propagation delay			
ECL to TTL	tp	typ.	4,50 ns
TTL to ECL	tp	typ.	2,40 ns
Power consumption per package	P_{av}	typ.	6,45 mW

FAMILY DATA see Family Specifications

PACKAGE OUTLINES (see chapter Package Outlines)

ORDERING INFORMATION
100255D: 16-lead DIL; ceramic (cerdip) (SOT-74B).

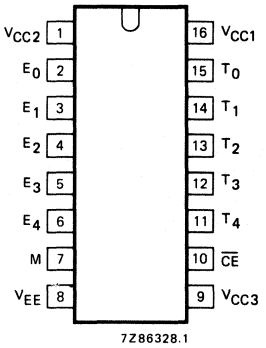


Fig. 2 Pin designation.

TRUTH TABLES

$\overline{CE}$	M	ECL input	TTL output
L	x	L	Z*
H	H	H	L
H	H	L	H

$\overline{CE}$	M	TTL input	ECL output
H	L	H	L
H	L	L	H

H = HIGH voltage level
L = LOW voltage level
x = Don't care
Z = High impedance TTL output
* = ECL output in OFF state; V_O = termination voltage V_T

RATINGS see family specifications.

D.C. CHARACTERISTICS

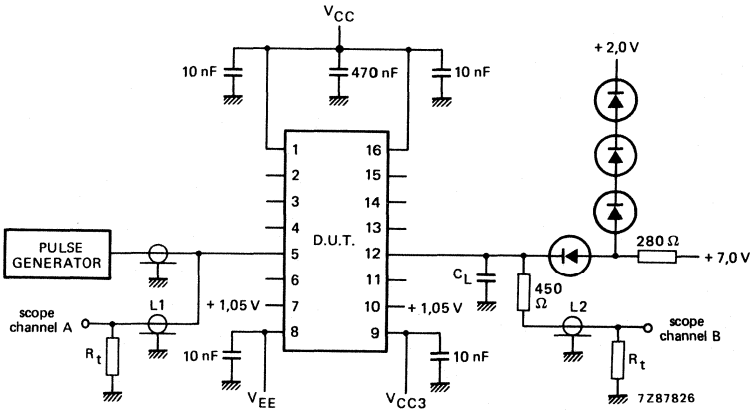
V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground; V_{CC3} = + 5 V; T_{amb} = 0 to + 85 °C;
device output load = 25 Ω to –2 V; unless otherwise specified

description	symbol	min.	typ.	max.	unit	remarks
ECL						
Input current LOW	I_{IL}	0,5	–	–	μA	Apply –1,81±0,005 V to each input in turn
Input current HIGH						
M, $\overline{CE}$	I_{IH}	–	–	350	μA	Apply –0,88±0,005 V to each input in turn
I/O	I_{IH}	–	–	350	μA	
Supply current	$-I_{EE}$	60	105	150	mA	For all modes
TTL						
Input current LOW I/O	I_{IL}	–1,6	–	–	mA	Apply +0,4 V to each input in turn and –0,88 V to $\overline{CE}$
Input current HIGH I/O	I_{IH}	–	–	40	μA	Apply +2,4 V to each input in turn and –0,88 V to $\overline{CE}$
Input breakdown current I/O	I_{IB}	–	–	1	mA	Apply +5,5 V to each input in turn and –0,88 V to $\overline{CE}$
Short circuit current	I_{OS}	–130	–	–40	mA	Apply –0,88 V to CE and M. Apply –1,81 V to one ECL I/O and V_{CC} = 0 V to the corresponding TTL I/O. Repeat for other channels
Output current for TTL output in high impedance state:						
high level output	I_{OZH}	–	–	40	μA	Apply +2,4 V to TTL I/O; other inputs open
low level output	I_{OZL}	–40	–	–	μA	Apply +0,4 V to TTL I/O; other inputs open
Supply current HIGH	I_{CCH}	25	35	44	mA	Apply –0,88 V to $\overline{CE}$, M and ECL I/O. TTL I/O open
Supply current LOW	I_{CCL}	19	27	36	mA	Apply –0,88 V to $\overline{CE}$ and M; apply –1,81 V to TTL I/O. TTL I/O open
Output voltage HIGH	V_{OH}	2,4	–	–	V	Loading = 2 mA; V_{CC3} = 4,75 V
Output voltage LOW	V_{OL}	–	–	0,4	V	Loading = 20 mA; V_{CC3} = 4,75 V
Input voltage clamp	V_{IC}	–1,5	–	–	V	Input current = 12 mA V_{CC3} = 4,75 V

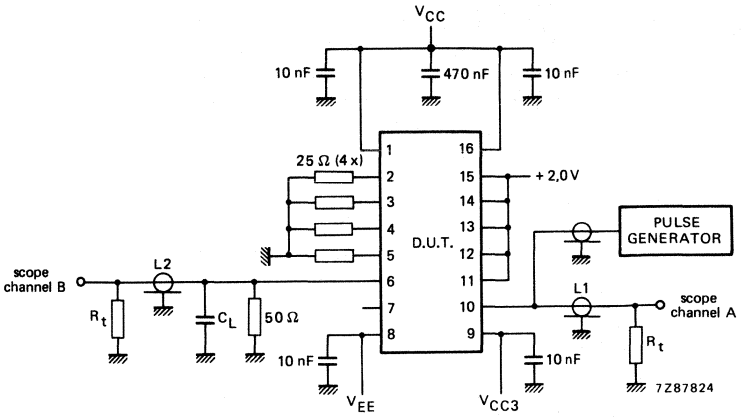
A.C. CHARACTERISTICS

V_{EE} = –4,2 to –4,8 V; V_{CC1} = V_{CC2} = ground; V_{CC3} = + 5 V; ECL 100 K output load = 25 Ω to –2 V

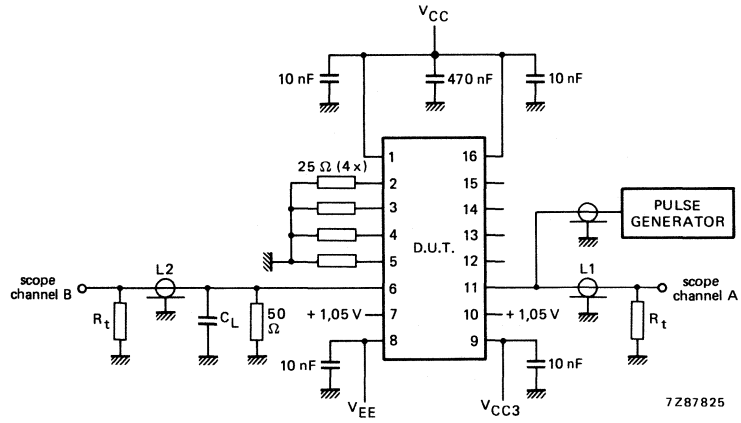
description	symbol	0°C		+25°C		+85°C		unit	remarks
		min.	max.	min.	max.	min.	max.		
Propagation delay									
ECL I/O to TTL I/O	t_{PLH} t_{PHL}	–	7	–	7	–	7	ns	see Figs 3 and 4
TTL I/O to ECL I/O	t_{PLH} t_{PHL}	–	8	–	8	–	8	ns	see Figs 3 and 5
$\overline{CE}$ to ECL I/O	t_{PLH} t_{PHL}	–	8	–	8	–	8	ns	see Figs 3 and 6
Transition time ECL	t_{PLH} t_{PHL}	0,75	–	0,75	–	0,75	–	ns	see Fig. 5
Transition time TTL	t_{PLH} t_{PHL}	0,75	–	1	–	1	–	ns	see Fig. 4



(a) ECL to TTL



(b) ECL to ECL



(c) TTL to ECL

Fig. 3 Switching time test circuit.

Notes:

$V_{CC1} = V_{CC2} = +2$ V; $V_{CC3} = +7$V; $V_{EE} = -2,5$ V;
$L_1 = L_2 = 50\ \Omega$ impedance lines of equal length;
$R_t = 50\ \Omega$ termination to scope.
Decoupling 0,01 μF from ground to V_{CC} and V_{EE};
C_L = fixture + stray capacitance $\leqslant 3$ pF.

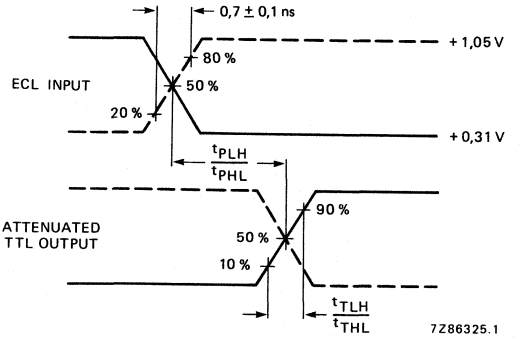


Fig. 4 ECL to TTL interface waveforms.

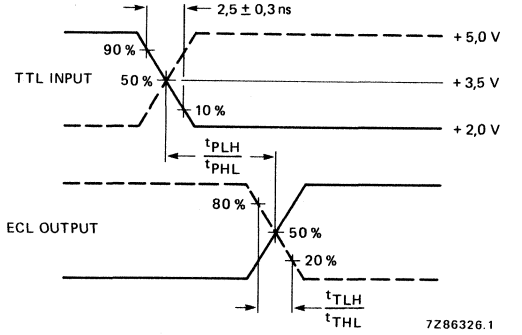


Fig. 5 TTL to ECL interface waveforms.

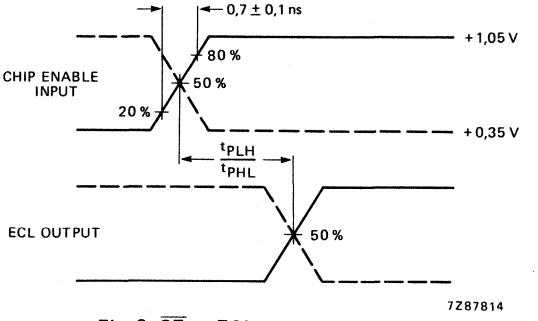


Fig. 6 $\overline{CE}$ to ECL output waveforms.

ACE FAMILY SPECIFICATIONS

ADVANCED CUSTOMIZED ECL (ACE)

INTRODUCTION

The Advanced Customized ECL (ACE) logic cell array family has the high performance and functional capability of ECL LSI without the costs and turn-around times inherent with full custom logic. The arrays of this family are especially suitable for mainframe computers, but can also be used in any high-speed digital system.

Using CML (Current Mode Logic) internally, with ECL (Emitter Coupled Logic) voltage compensated 10KH or 100K I/O translation, equivalent gate speeds are down to 0,35 ns. Combined with an equivalent gate current consumption of 500 μA this results in internal speed power products reaching 1 pico-joule. By use of an external resistor the I/O cells of ACE arrays can directly drive TTL gates.

The gate complexity ranges from 600 to 2200 gates. The arrays are organized into internal cell sites (24 to 100) and peripheral sites. A standard cell library with complete CAD package facilitates quick, economical and error-free realization of a wide range of LSI logic functions.

External I/O voltage levels and supply voltage requirements make the devices fully compatible with either the 10KH or 100K ECL family, or even with TTL logic levels with an external pull-up resistor.

FEATURES

- family of semi-custom LSI
- 10KH or 100K compatibility
- very high speed
- low power dissipation
- bidirectional I/Os
- 25 Ω drive ability
- TTL drive compatible
- pin grid array packaging
- air cooled arrays

APPLICATIONS

- large mainframe CPU
- high speed peripherals
- telecommunications
- instrumentation
- signal processing
- data communications

QUICK REFERENCE DATA

			10KH	100K	
Supply voltage (± 5%)	V_{EE}	typ.	−5,2	−4,5	V
Standard load conditions	R_L	typ.	50	50	Ω
Propagation delay per equivalent gate					
SSI	t_{pd}	typ.	0,50		ns
MSI	t_{pd}	typ.	0,35		ns
LSI	t_{pd}	typ.	0,45		ns
Junction temperature	T_j	max.	+ 150		°C
Storage temperature range	T_{stg}		−65 to + 150		°C

PRODUCT DESCRIPTION

The present ACE family consists of five arrays ACE600, ACE900, ACE1400, ACE2200 and ACE1320M. The last one including on-chip RAM.

ACE is a semi-custom family with macro function cell structure. A dedicated LSI circuit is made by implementation of an interconnection pattern provided by the combination of several macro functions selected from a fully specified cell library. The interconnection pattern is made by two metal layers.

The ACE family uses a well-proven 5 GHz oxide-isolated process, fully implanted, with walled emitters. The internal I/O sites can be defined as input, output or bidirectional I/O devices. Output cells have mask programmable transition times to ease printed-circuit designs. They can be configured as TTL transceivers with an external resistor. The arrays are 10KH or 100KH compatible by mask option. Multiple supply pins maintain high noise immunity.

description	ACE600	ACE900	ACE1400	ACE2200	ACE1320M
Chip size mil^2	43 400	55 800	85 200	120 000	104 000
mm^2	28	36	55	77,4	67
Logic cell sites	24	36	60	100	52
Input cell sites	30	30	–	–	–
I/O cell sites	28	28	96	128	112
Equivalent gates					
typical	450	650	1050	1600	700
maximum	600	900	1400	2200	1000
Connection channels					
first layer	52	72	108	164	136
second layer	52	52	96	96	96
overcells	30	30	50	50	50
Number of pins	64	64	144	144	144
Supply pins	6	6	16	16	16
On-chip RAM	–	–	–	–	320 bits

CODE IDENTIFICATION

(ordering information)

referenced array	10K ECL	100K ECL	suffix for packages	
			without heatsink	with heatsink
ACE600	22-XXX	221-XXX	PB	PBH
ACE900	23-XXX	231-XXX	PB	PBH
ACE1400	24-XXX	241-XXX	PBK	PBKH
ACE2200	25-XXX	251-XXX	PBK	PBKH
ACE1320M	26-XXX	261-XXX	PBK	PBKH

XXX digits are assigned during code development phase.

MAXIMUM THERMAL CHARACTERISTICS

Circuit with heatsink mounted in a test socket and transverse air flow ⩾ 5 m/s is maintained.
64-pin package: 7 K/W
144-pin package: 5 K/W

PACKAGE OUTLINE

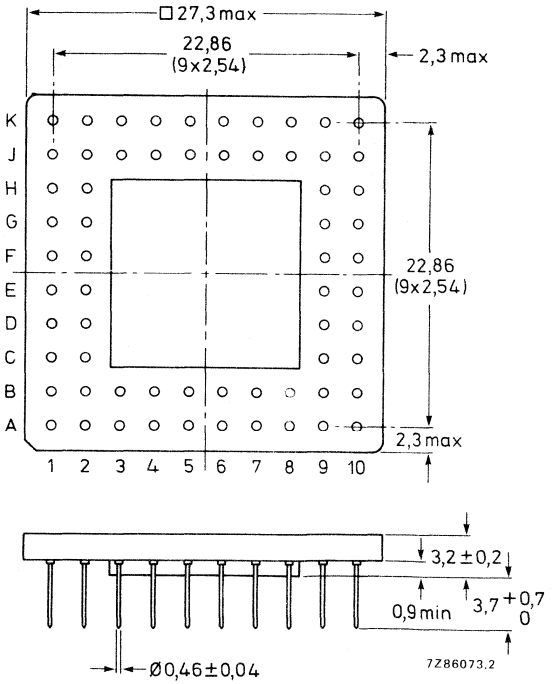


Fig. 1 64-pin plug-in package (FO-75) for ACE600 and ACE900.

DEVELOPMENT SAMPLE DATA

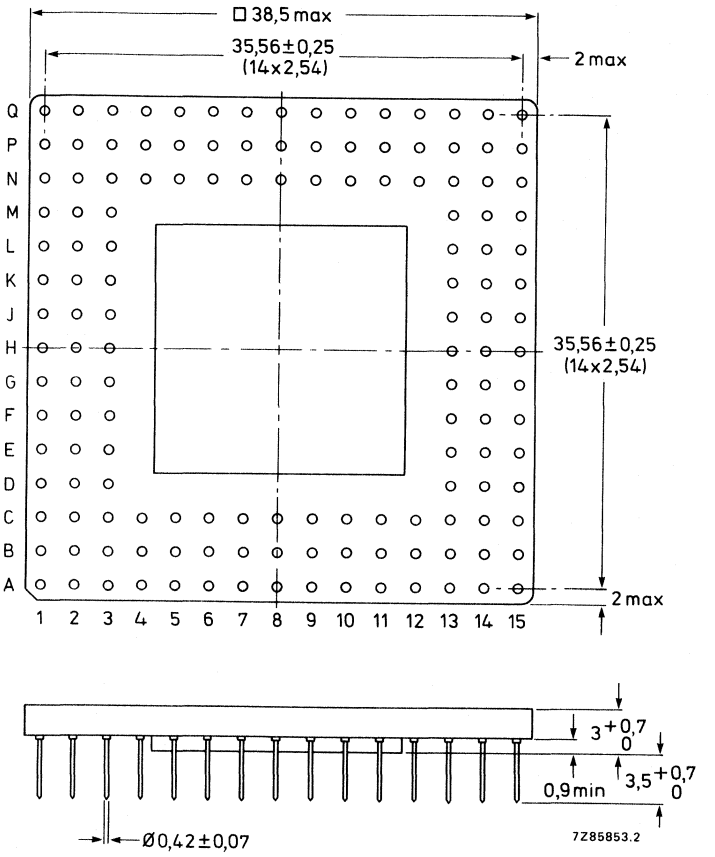


Fig. 2 144-pin plug-in package (FO-108) for ACE1320M, 1400 and 2200.

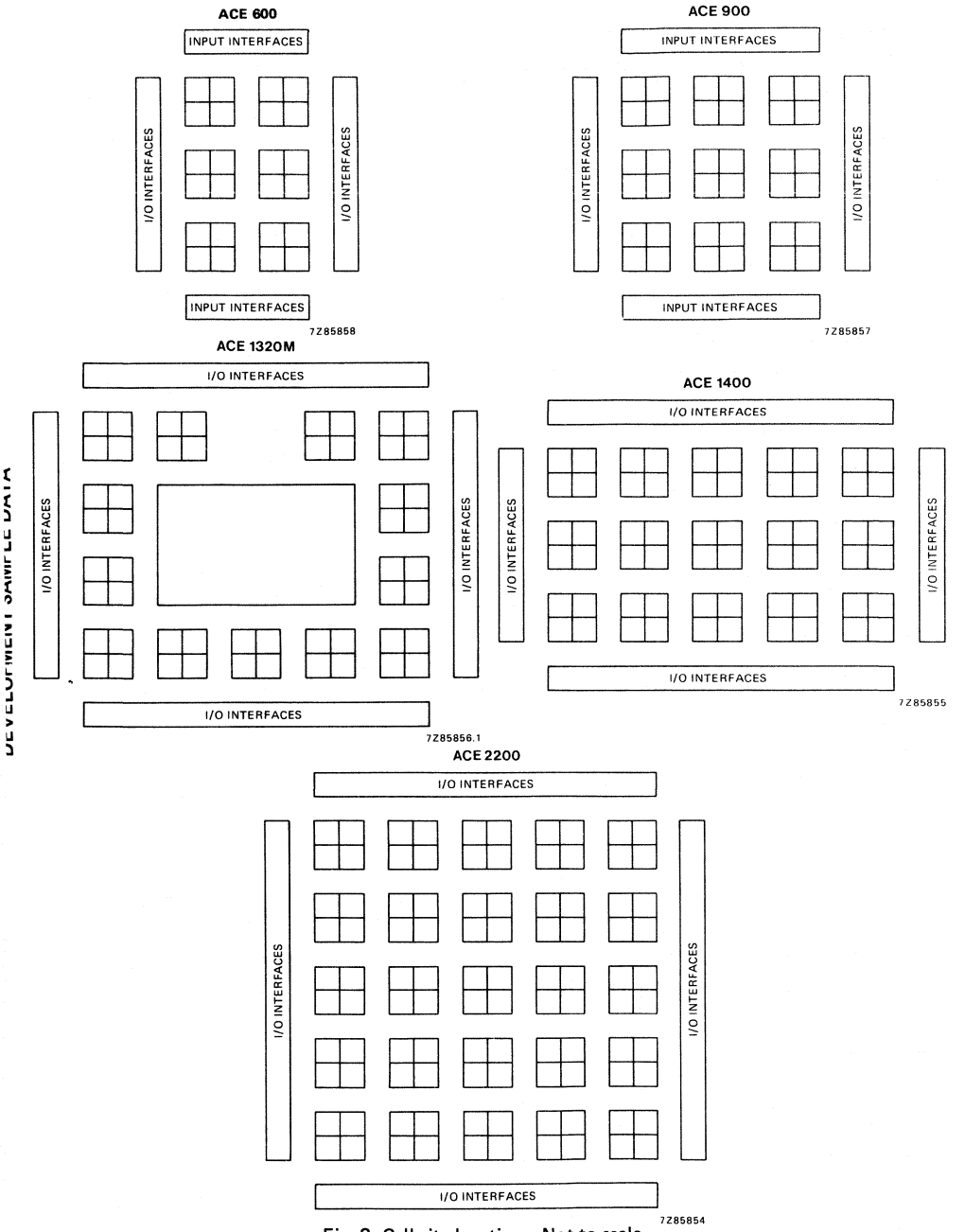


Fig. 3 Cell site locations. Not to scale.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$-V_{EE}$	max.	7 V
Input voltage (d.c.) range	V_I		0 to V_{EE} V
		min.	−6 V
D.C. output current	I_O	max.	50 mA
Pulsed output current t_p = 10 μs; δ = 1%	I_{OP}	max.	100 mA
Junction temperature	T_j	max.	+ 150 °C
Storage temperature range	T_{stg}		−65 to + 150 °C

D.C. CHARACTERISTICS

$V_{CC1} = V_{CC2} = 0$ V (ground); $R_L = 50\ \Omega$ to $V_{TT} = -2$ V

Input current at V_{IL}	I_{IL}	min.	0,5 μA
at V_{IH}	I_{IH}	max.	265 μA
Supply current*	I_{EE}	min.	0,7 x $I_{EE\,typ}$
		max.	1,4 x $I_{EE\,typ}$

- **At standard load of 50 Ω to $V_{TT} = -2$ V**

at junction temperature of		10KH 30 °C	10KH 60 °C	10KH 125 °C	100K 30 to 125 °C
Supply voltage (± 5%)	V_{EE}	−5,2	−5,2	−5,2	−4,5 V
Output voltage HIGH	V_{OHmin}	−1,02	−0,98	−0,91	−1,025 V
	V_{OHmax}	−0,84	−0,81	−0,72	−0,88 V
Output voltage LOW	V_{OLmin}	−1,95	−1,95	−1,95	−1,81 V
	V_{OLmax}	−1,63	−1,63	−1,59	−1,62 V
Input voltage HIGH	V_{IHmin}	−1,17	−1,13	−1,06	−1,165 V
Input voltage LOW	V_{ILmax}	−1,48	−1,48	−1,44	−1,475 V

- **Load 25 Ω to $V_{TT} = -2$ V**

at junction temperature of		10KH 30 °C	10KH 60 °C	10KH 125 °C	100K 30 to 125 °C
Output voltage HIGH	V_{OHmin}	−1,07	−1,03	−0,96	−1,075 V
	V_{OHmax}	−0,84	−0,81	−0,72	−0,880 V
Output voltage LOW	V_{OLmin}	−1,95	−1,95	−1,95	−1,810 V
	V_{OLmax}	−1,63	−1,63	−1,59	−1,620 V

- **In case of line receivers**

Differential voltage	V_D	min.	150 mV
Common mode voltage	V_{CM}	min.	−2,0 V
Input voltage HIGH	V_{IH}	max.	−0,6 V
		min.	−2,0 V
Input voltage LOW	V_{IL}	min.	V_{EE} V

* Typical supply current ($I_{EE\,typ.}$) is code related, computed by ACELOR program.

A.C. CHARACTERISTICS

Internal propagation delay per equivalent gate

SSI	t_{pd}	typ.	0,50 ns
MSI	t_{pd}	typ.	0,35 ns
LSI	t_{pd}	typ.	0,45 ns

Typical propagation delays (t_{pd}) are defined in the cell library for every function:

$t_{pd\ max} = 1{,}4 \times t_{pd\ typ}$
$t_{pd\ min} = 0{,}6 \times t_{pd\ typ}$

This is including process, temperature and supply voltage variations.

Output transition time (Fig. 5)		slow	standard	fast	
minimum mask option	$t_{THL/TLH}$	0,7	0,5	0,4	ns
typical mask option	$t_{THL/TLH}$	1,4	1,0	0,8	ns
maximum mask option	$t_{THL/TLH}$	2,5	2,0	2,0	ns

Conditions for a.c. test		10KH	100K	
Ground	V_{CC1}, V_{CC2}	+ 2	+ 2	V
Supply voltage	V_{EE}	−3,2	−2,5	V
Input voltage HIGH	V_{IH}	V_{CC}−0,890	V_{CC}−0,955	V
Input voltage LOW	V_{IL}	V_{CC}−1,690	V_{CC}−1,705	V
Output load to ground	R_L	50	50	Ω
Input pulse transition times	$t_{THL/TLH}$	1,5	0,7	ns

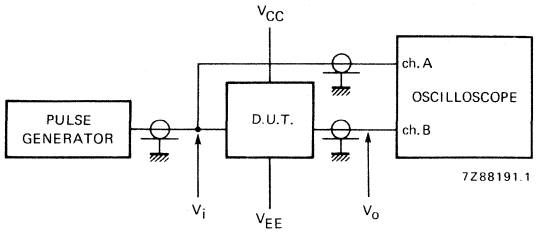


Fig. 4 Switching times test circuit.

$V_{CC1} = V_{CC2} = +2$ V; input and output connections are 50 Ω cables; oscilloscope input impedance = 50 Ω; $V_{EE} = -2{,}5$ V for 100K ECL or −3,2 V for 10KH ECL devices.

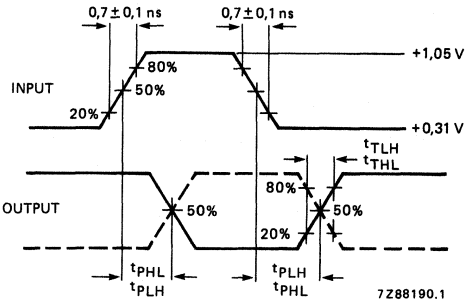


Fig. 5 Switching times waveform.

		10KH devices	100K devices
Input voltage HIGH	V_{IH}	+ 1,11 V	+ 1,045 V
Input voltage LOW	V_{IL}	+ 0,31 V	+ 0,295 V
Transition time	$t_{TLH/THL}$	1,5 ns	0,7 ns

Notes

1. A cell with TTL drive ability can be implemented on every I/O site and with a load resistor connected to + 5 V it can drive any TTL device. This cell can be bidirectional; the output is equivalent to an open collector output with a clamping voltage of about 3 V; the input being equivalent to a TTL input with a higher input current. The d.c. and a.c. characteristics of this cell, as well as computation of load resistor are described in ACE USER'S GUIDE.
2. ACE1320M includes on-chip RAM. The RAM is configured in two blocks of 16 words of 10 bits. It can be reconfigured by mask options as 64 words by 5 bits or 16 words by 20 bits. Address access time (t_{AA}) typical 3,5 ns, maximum 5,5 ns.

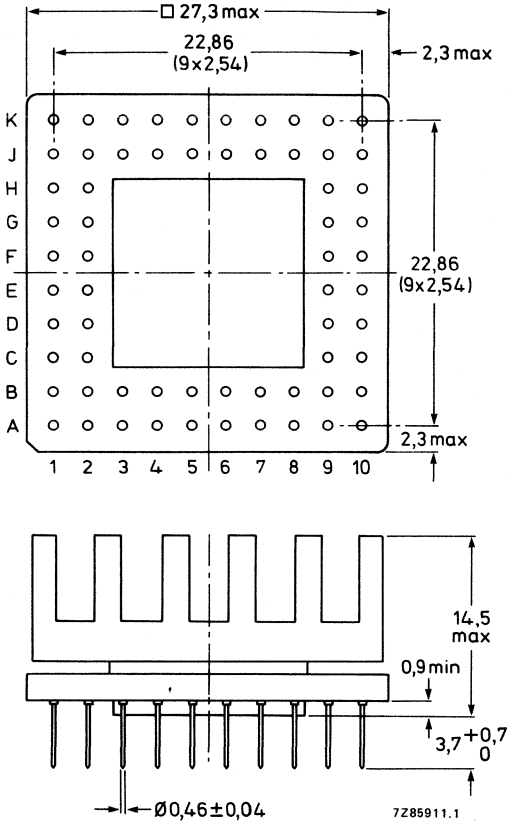


Fig. 6 Mechanical data FO-99 (FO-75 with heatsink). Dimensions in mm.

MAXIMUM THERMAL RESISTANCE

Package mounted on a printed circuit board.

	$R_{th\ j\text{-}a}$ (K/W)	
	with air flow*	without
FO-99	7	20
FO-75	25	50

* Forced air flow of 5 m/s (= 1000 linear f/min).

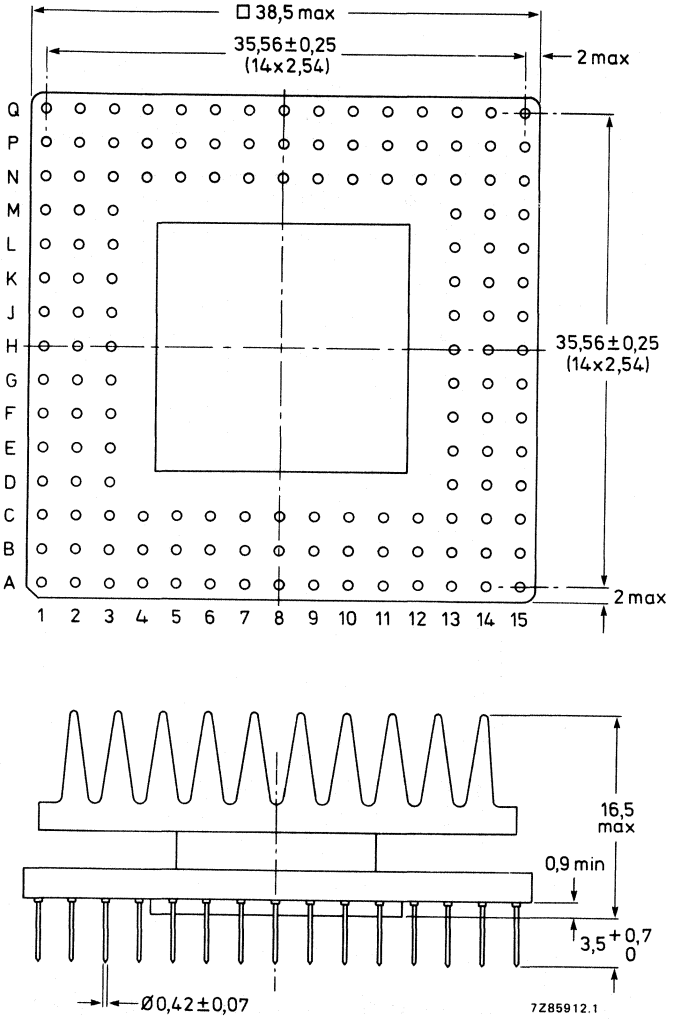


Fig. 7 Mechanical data FO-128 (FO-108 with heatsink). Dimensions in mm.

MAXIMUM THERMAL RESISTANCE

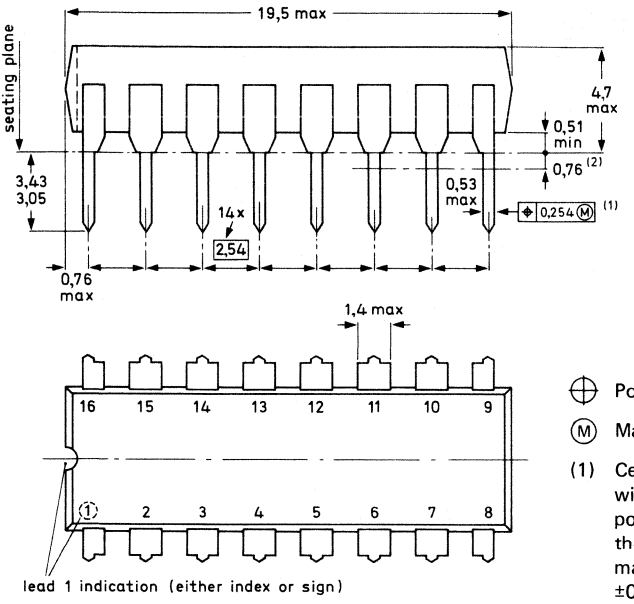
Package mounted on a printed circuit board.

	$R_{th\ j\text{-}a}$ (K/W)	
	with air flow *	without
FO-128	5	15
FO-108	15	30

* Forced air flow of 5 m/s (= 1000 linear f/min).

PACKAGE OUTLINES

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

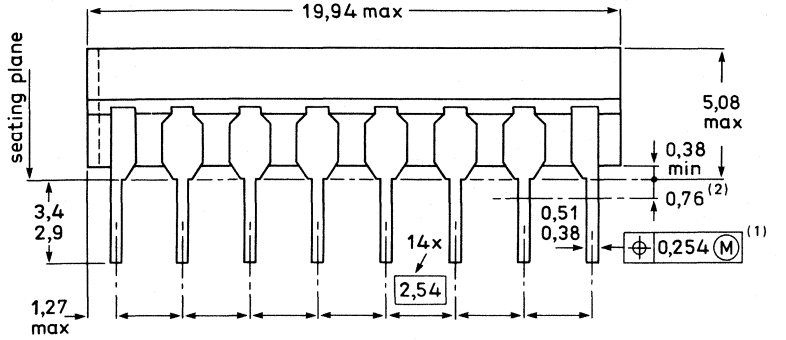
2. By dip or wave

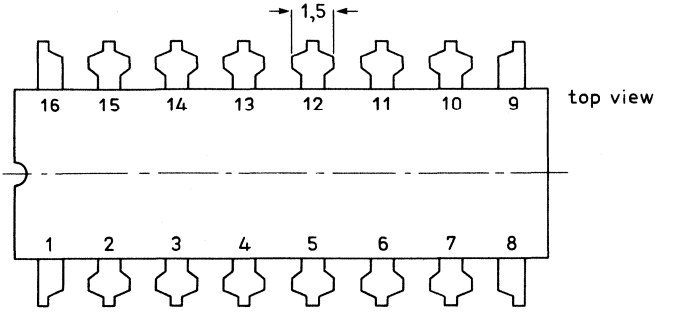
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

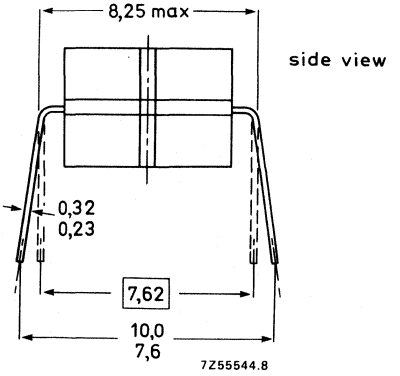
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-74A,B,C)







⊕ Positional accuracy.

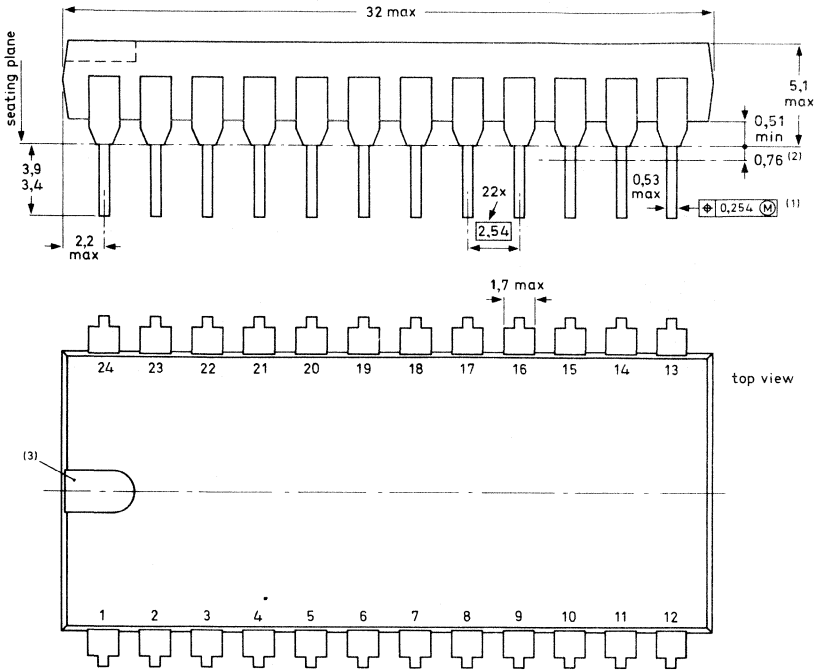
Ⓜ Maximum Material Condition.

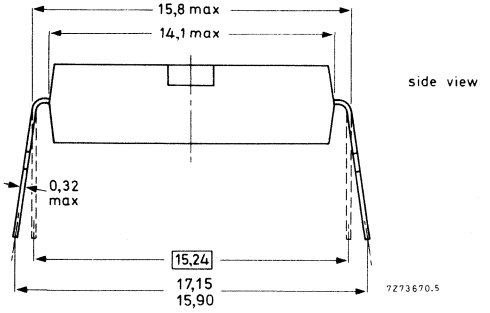
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

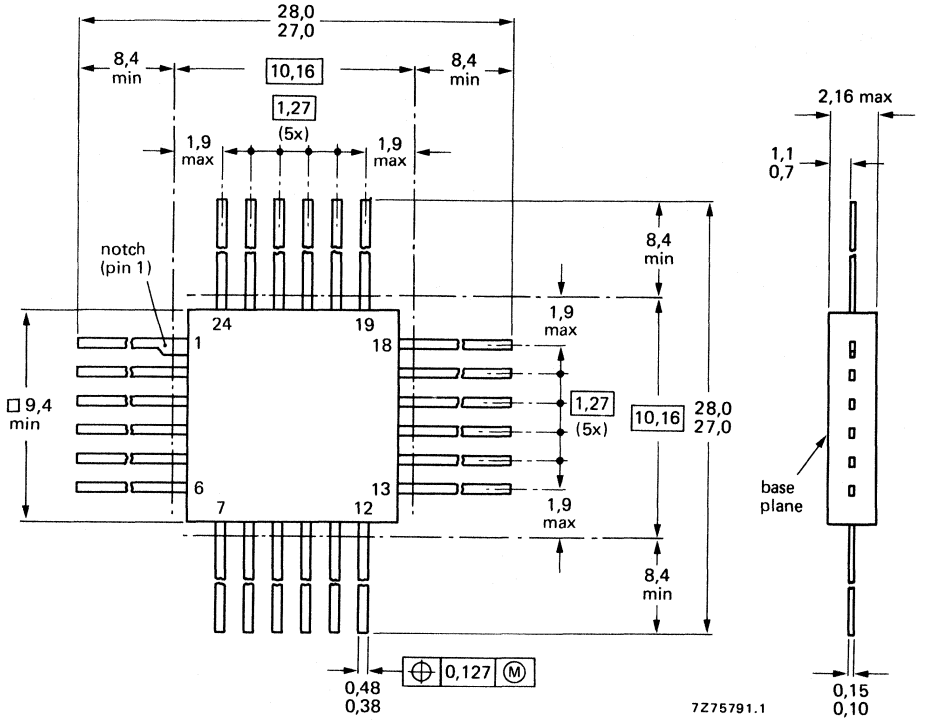
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

24-LEAD FLATPACK; CERAMIC (SOT-138)



Dimensions in mm

Pins are tin-plated nickel alloy.

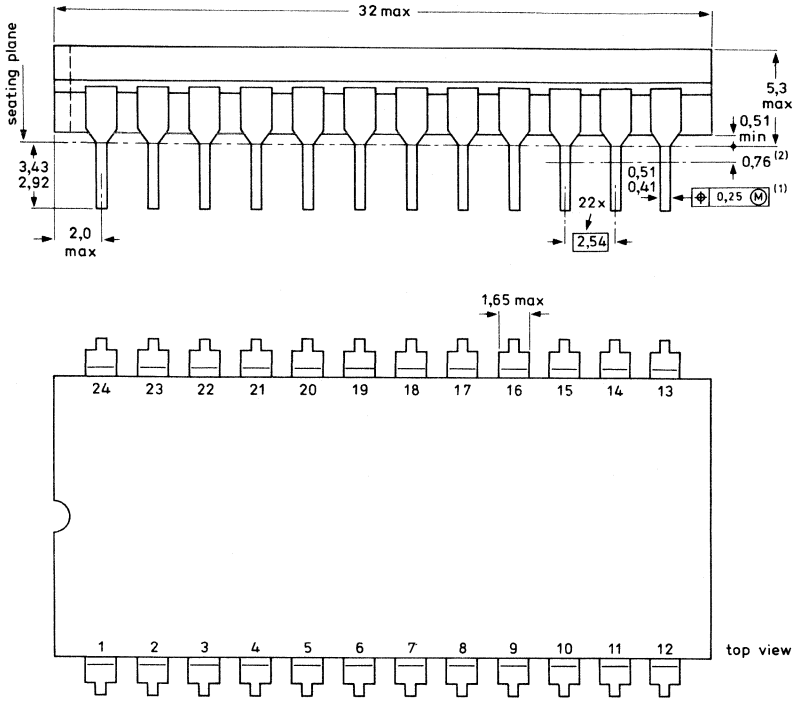
Base is Al_2O_3 or BeO (toxic material).

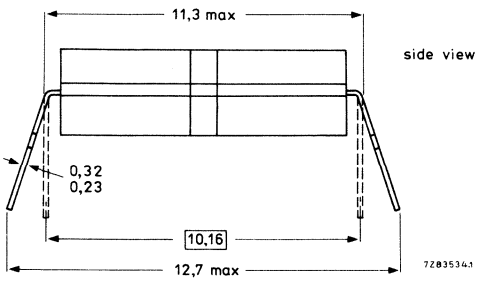
Mass = 0,8 g.

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

24-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT-149)





⊕ Positional accuracy.

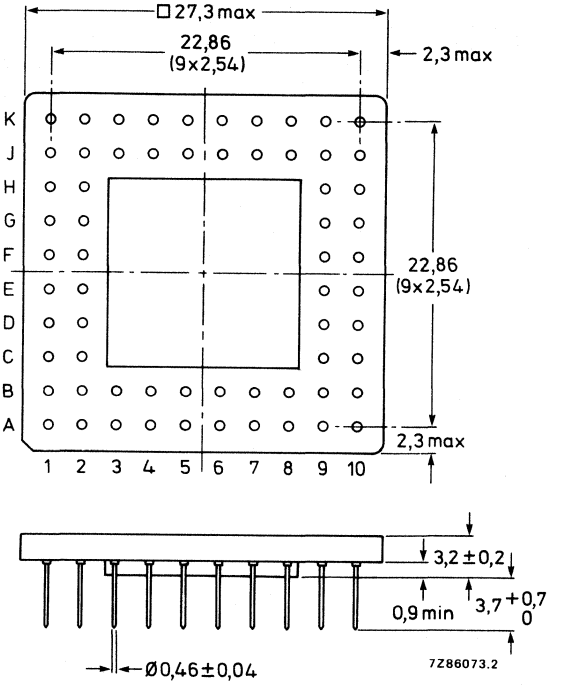
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

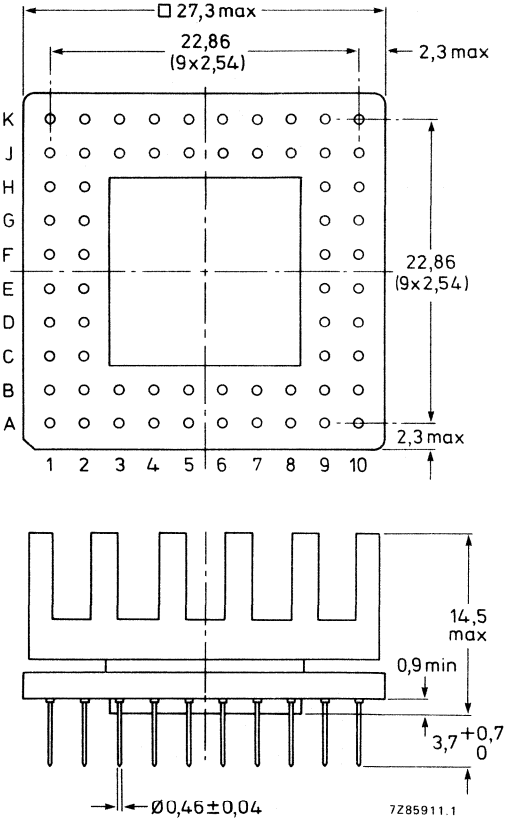
Dimensions in mm

64-PIN PLUG-IN PACKAGE (FO-75)



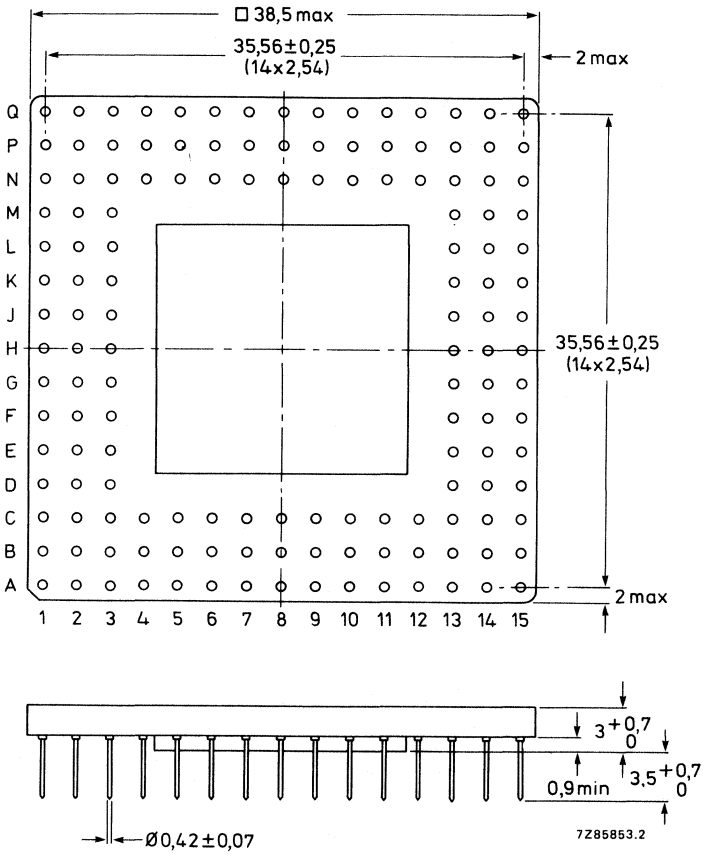
Dimensions in mm

64-PIN PLUG-IN PACKAGE WITH HEATSINK (FO-99)



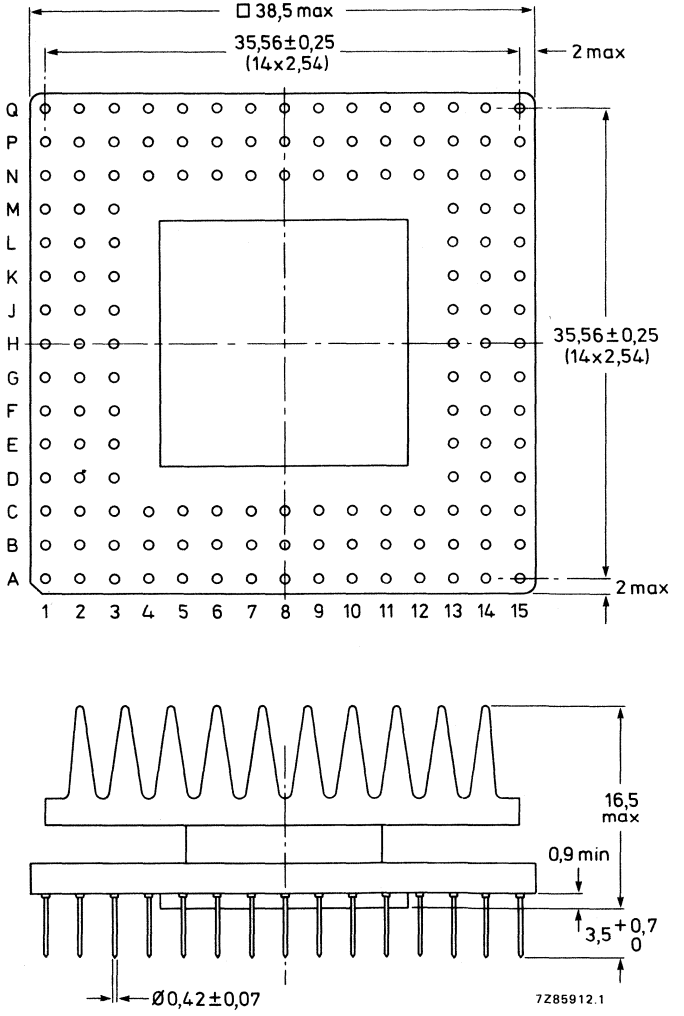
Dimensions in mm

144-PIN PLUG-IN PACKAGE (FO-108)



Dimensions in mm

144-PIN PLUG-IN PACKAGE WITH HEATSINK (FO-128)



Dimensions in mm

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